DATA BOOK

Communications

MEDICAL APPLICATIONS

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CROSS REFERENCE GUIDE

Vendor	P/N	Description	UMC/PN
THOMSON MOSTEK	MK5087	Tone Dialer	*UM95087
THOMSON MOSTEK	MK5089	Tone Dialer	*UM95089
THOMSON MOSTEK	MK5092/5094	Tone Dialer	UM95088
THOMSON MOSTEK	MK50981	Pulse Dialer	UM9151-3
THOMSON MOSTEK	MK50982	Pulse Dialer	UM9151-3
THOMSON MOSTEK	MK50992	Pulse Dialer	UM9151-3
THOMSON MOSTEK	MK50993	Pulse Dialer	UM9151-3
THOMSON MOSTEK	MK5173	10 Memory Pulse Dialer	UM91611
THOMSON MOSTEK	MK5175	10 Memory Pulse Dialer	UM91611
THOMSON MOSTEK	MK5175/5380	10 Memory T/P Dialer	UM91260/61
THOMSON MOSTEK	MK5375	10 Memory T/P Dialer	UM91260/61
THOMSON MOSTEK	MK5380	Tone Dialer	UM95088
AMI	S25089	Tone Dialer	*UM95089
AMI	S2559E/F	Tone Dialer	*UM9559E/F
AMI	S2560	Pulse Dialer	UM9151-3
AMI	S25610	10 Memory Pulse Dialer	*UM91611
AMI	S25910	10 Memory T/P Dialer	UM91260/61
AMI	S2859	Tone Dialer	UM95088
AMI	S2860	Tone Dialer	UM95088
MOTOROLA	MC145410	10 Memory T/P Dialer	UM91260/61
TI	TCM1101	Pulse Dialer	UM9151-3
TI	TCM5087	Tone Dialer	*UM95087
TI	TCM5089	Tone Dialer	*UM95089
TI	TCM5092	Tone Dialer	UM95088
NS	TP5087	Tone Dialer	*UM95087
NS	TP5089	Tone Dialer	*UM95089
NS	TP53144	Pulse Dialer	UM9151-3
NS	TP53190	Pulse Dialer	UM9151-3

*Pin to Pin Compatible

Vendor	P/N	Description	UMC/PN
NS	TP5393	Pulse Dialer	UM9151-3
NS	TP5395	Tone Dialer	UM95088
NS	TP5605	10 Memory Pulse Dialer	UM91611
NS	TP5615	10 Memory Pulse Dialer	UM91611
NS	TP5660	10 Memory T/P Dialer	UM91260/61
SHARP	LR40992	Pulse Dialer	UM9151-3
SHARP	LR40993	Pulse Dialer	UM9151-3
SHARP	LR4173	10 Memory Pulse Dialer	UM91611
SHARP	LR4087	Tone Dialer	*UM95087
SHARP	LR4089	Tone Dialer	UM95089
SHARP	LR48081	Tone/Pulse Dialer	UM91210
SHARP	LR4803	10 Memory T/P Dialer	UM91260/61
SHARP	LR4806	20 Memory T/P Dialer	UM91270
SEIKO	S7230/5	Tone/Pulse Dialer	*UM91230
SEIKO	S7241	20 Memory T/P Dialer	UM91271
SEIKO	STC2580	10 Memory T/P Dialer	UM91260/61
ROHM	BU8320	20 Memory T/P Dialer	UM91270
SANYO	LC7350	Pulse Dialer	UM9151-3
SANYO	LC7360/3	Tone/Pulse Dialer	UM91210
SANYO	LC7365	Tone Dialer	UM95088
SANYO	LC7366	Tone Dialer	UM95089
OKI	MSM5070/IRS	Tone/Pulse Dialer	UM91210
OKI	MSM6224	Tone Dialer	UM95088
OKI	MSM6234	Tone Dialer	*UM95089
ERSO	CIC9145	15 Memory Tone/Pulse Dialer	*UM91265
Philips	PCD3310	Tone/Pulse Dialer	*UM91310

*Pin to Pin Compatible

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SELECTION TABLE

Feature	Pulse	Tone/Pulse	Tone
Simple (without redial)			UM9559E/F UM95087/88/89
Simple (with redial)	UM9151 UM9151-3	UM91210/30 UM91214/15	
10 Memory (indirect dialing)	UM91611	UM91260/61	
15 Memory (direct + indirect dialing)		UM91265	
20 Memory (direct dialing)		UM91270 UM91271/72	

Pulse Dialer

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UM9151

Pulse Dialer

Features

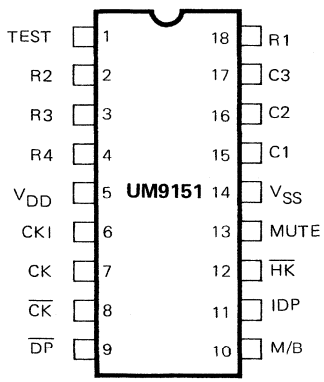
- Direct telephone line operation
- 4 x 3 matrix single contact keyboard
- Supply voltage range of 2.5 to 5.0 volts
- Uses inexpensive RC oscillator
- Low power standby mode for redialing
- 22-digit redialing capacity
- Redialing with either * or # key
- Dialer reset for line power breaks > 200 ms
- Pin-selectable inter-digital pause
- Pin-selectable make/break ratio
- High speed testing capacity

General Description

The UM9151 pulse dialer is a monolithic CMOS integrated circuit which converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended to replace mechanical telephone dialers and can operate directly from telephone lines. The pulse dialer function is implemented using two outputs; one pulses the line, the other mutes the receiver.

CMOS technology is used to produce this device, resulting in very low power requirements and high noise immunity. The UM9151 can be easily interfaced with a variety of telephones, requiring only a minimum number of external components.

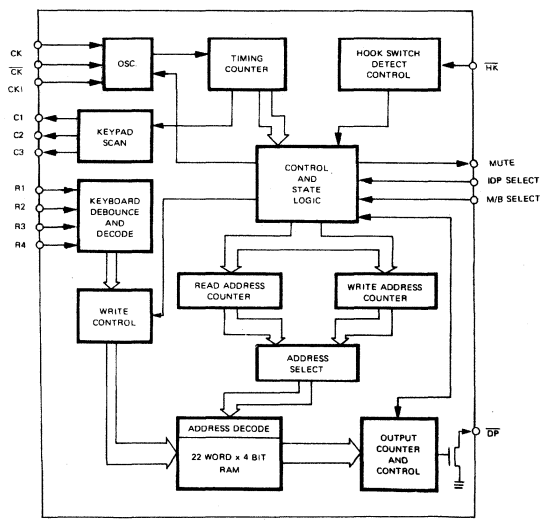
Pin Configuration & Keyboard Assignments



1	2	3
4	5	6
7	8	9
*	0	#

(* #: Redial)

Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage ($V_{DD}-V_{SS}$) . . . . . –0.3V to 6.0V

Input Voltage (V_{IN}) . . . . . –0.3V to V_{DD} + 0.3V

Maximum Power Dissipation (at 25°C) . . . . . 600 mW

Operating Temperature (T_{OP}) . . . . . –20°C to +70°C

Storage Temperature (T_{STG}) . . . . . –55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Test Ckt
DC Supply Voltage	V_{DD}	2.5	–	5	V		A
Supply Current Standby	I_S	–	–	1	μA	V_{DD} = 2.5V with pins 1, 10, 11 connected	A
Operating	I_D	–	–	150	μA	V_{DD} = 5V pin 9 open	A
Keyboard Contact Resistance Capacitance	 R C	 – –	 – –	 1 30	 KΩ pF		
MUTE Sink Current	I_{MS}	500	–	–	μA	V_{DD} = 2.5V, V_O = 0.5V	B
MUTE Driving Current	I_{MD}	500	–	–	μA	V_{DD} = 2.5V, V_O = 2V	B
$\overline{DP}$ Sink Current	I_{LS}	500	–	–	μA	V_{DD} = 2.5V, V_O = 0.5V	B
$\overline{DP}$ Leakage Current	I_{LL}	–	–	1	μA	V_{DD} = 5V, V_O = 5V	B

AC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, clock freq. = 18KHz, T_{OP} = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PULSE						
Make/Break Ratio	M/B	M/B = V_{DD}	–	1/2	–	
		M/B = V_{SS}	–	2/3	–	
Dial Pulse Rate	DR	V_{DD} = 3.5V, F_{OSC} = 18KHz	–	10	–	PPS
Make Time	T_M	M/B = V_{DD}	–	33.3	–	ms
		M/B = V_{SS}	–	40	–	
Break Time	T_B	M/B = V_{DD}	–	66.6	–	ms
		M/B = V_{SS}	–	60	–	
Inter-digital Pause Time	T_{IDP}	IDP = V_{DD}	–	500	–	ms
		IDP = V_{SS}	–	800	–	

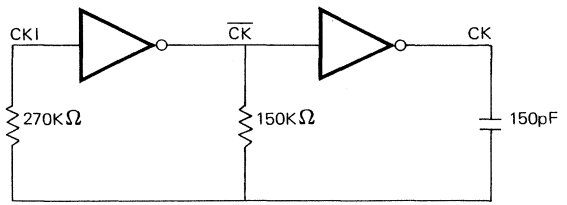
AC Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Pre-digital Pause	T_{PDP}	IDP = V_{DD}	–	500	–	ms
		IDP = V_{SS}	–	800	–	
MUTE Delay Time	T_{MDP}	M/B = V_{DD}	–	33.3	–	ms
		M/B = V_{SS}	–	40	–	
KEY-IN						
Keyboard Debounce Time	T_{KD}	V_{DD} = 3.5V, F_{OSC} = 18KHz	–	6.7	–	ms
Key Scan Frequency	F_{KS}			200		Hz
Oscillation Frequency	F_{OSC}	Per typical application V_{DD} = 3.5V		18		KHz
Frequency Variation vs. Voltage	ΔF/F	V_{DD} = 2.5 ~ 3.5V, $(F_{3.5} - F_{2.5})/F_{3.5}$	0	–	+4	%
	ΔF/F	F_{DD} = 3.5 ~ 5V, $(F_5 - F_{3.5})/F_5$	0	–	+4	%
Frequency Variation per Lot	ΔF/F	Per typical application V_{DD} = 3.5V	–4	–	+4	%

Pin Description

Pin	Designation	Description
1	TEST	Test mode select input. Connecting this input to V_{SS} triggers the UM9151 into high speed test mode (dialing rate = 600 PPS).
18,2,3,4 15,16,17	R1 ~ R4 C1 ~ C3	Keyboard inputs. A pulse to logic low is sequentially switched around the three keyboard scan outputs, requiring 5 ms for a complete scan cycle. When a key is depressed, the pulse (logic low) appears on one of the four keyboard inputs (provided with on-chip pull-up resistors to logic high). Following key depression and 6.7 ms antibounce period, the data is entered to RAM. Before a second key depression can be recognized, the first key must be released and a full antibounce period completed without a pulse appearing on any input. If two or more keys are depressed during the same scan cycle, the data will be rejected and another full antibounce period must be completed without a pulse appearing on any of the inputs before the next key depression is recognized.
5	V_{DD}	Positive power supply input.
14	V_{SS}	Negative power supply input.

Pin Description (Continued)

Pin	Designation	Description
6,7,8	CKI,CK,$\overline{CK}$	Oscillator circuit inputs. To be connected to an RC oscillator. The oscillator consists of two inverters and external components which control the oscillation frequency. The circuit is sufficiently versatile to allow a variety of component combinations. The oscillation circuit detailed below has an oscillation frequency of 18KHz for 10 pps dialing rate.  Oscillator Circuit
9	$\overline{DP}$	Dialing pulse outputs. The loop-disconnect dial pulses appear at the $\overline{DP}$ output. This output consists of an N-channel open drain device sinking current to V_{SS}. During a dial pulse break period the output device is switched on and during the make period and IDP the output device is switched off. The output drives an external bipolar transistor that sequentially opens the telephone loop a number of times equal to the input digit selected. For example, key 7 will generate 7 loop current breaks.
10	M/B	Make/break ratio select input. When this input = V_{DD}, M/B ratio = 1:2. When this input = V_{SS}, M/B ratio = 2:3.
11	IDP	Inter-digital pause select input. When this input = V_{DD}, IDP = 500 ms. When this input = V_{SS}, IDP = 800 ms.
12	$\overline{HK}$	Hook switch input. External circuitry connected to the $\overline{HK}$ input is used to indicate whether the telephone handset is on-hook or off-hook, these two states being represented by logic HIGH and logic LOW respectively. If power is present on the dialer, this input should normally be held at logic LOW. If the $\overline{HK}$ input is taken to logic HIGH for a period of less than 200 ms and then returned to logic LOW, no action is taken and the dialer will continue to function. If it is taken to logic HIGH for a period greater than 200 ms, oscillator function and any dialing sequence will cease. All internal counters will be reset, though the contents of the RAM will be unaffected. Taking the input back to logic LOW will restart the keyboard scan and dialing sequence and dialer will be ready for a data entry.
13	MUTE	Mute output. This output consists of an inverter normally at low state when there is no key entry. The MUTE output is used to control the muting of the telephone network during outdialing. A logic HIGH indicates that the telephone is to be muted, the transition to logic HIGH occurring immediately on recognition of a key depression.

Operational Procedures

Symbol Definitions:

DP: pulse digit (0 through 9).
ZiZiZi: conversation.
0-0 ↑: off-hook.
0-0 ↓: on-hook.

Recommended Operations:

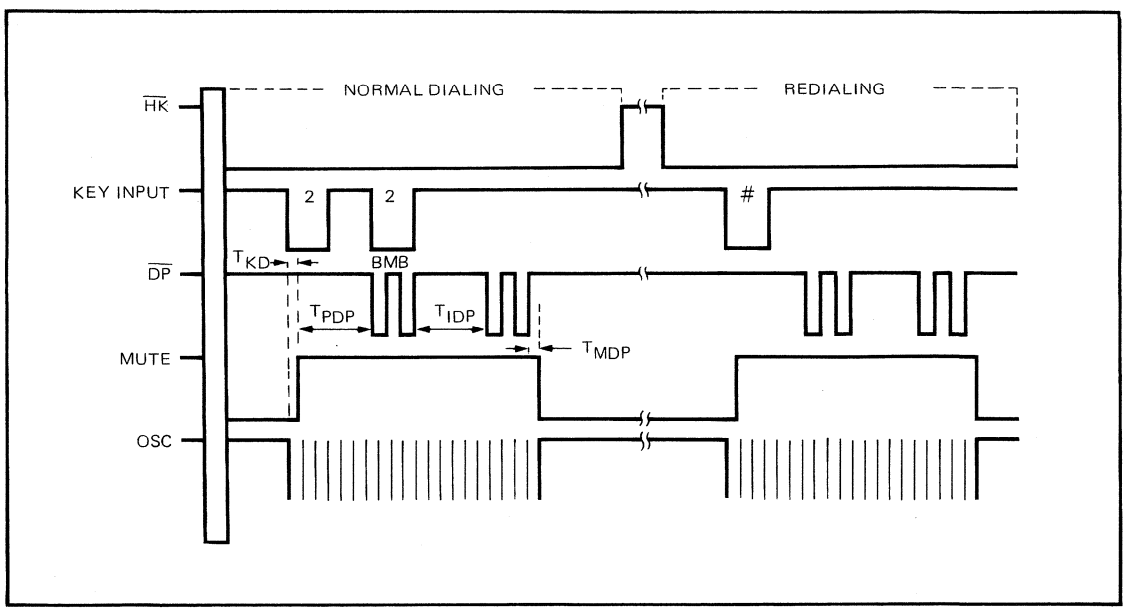
* Normal dialing:
  0-0 ↑: DP . . . Dp; ZiZiZi; 0-0 ↓.
* Redialing:
  0-0 ↑; * or # key; . . .

Note: Redialing

Keyboard inputs are accepted at an asynchronous rate and loaded into a first-in-first-out RAM. If a call is not successful, it can be redialed at a later time by pressing either of the redial keys, * or #. The correct number of pulses will then be read out a second time.

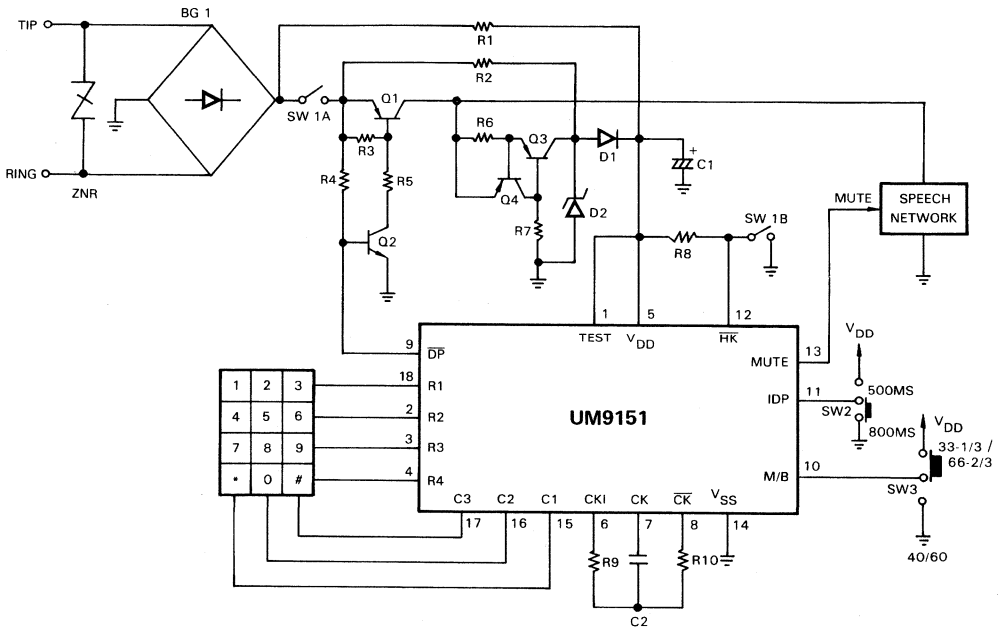
Since the UM9151 allows one key to be entered before pressing a redial key, it is suitable for use in PABX systems.

Timing Diagram



Typical Application

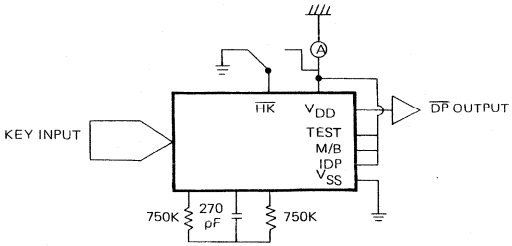
An example of a loop disconnect UM9151 interface:



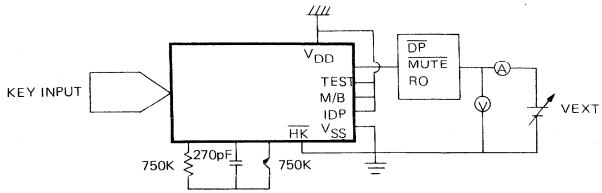
Circuit Description	Parts List
1. Loop Disconnect Interface: Q_1, Q_2, R_3, R_4, R_5 and $\overline{DP}$ Q_1 and Q_2 act as switching transistors, $\overline{DP}$ is the dial pulse output which drives Q_2 transistor on and off as make and break, R_4 pulls up the $\overline{DP}$ output, R_3 protects the Q_1 transistor during break period and R_5 limits the base current of Q_1. **2. Power supply: R_1, R_2, R_6, R_7, Q_3, Q_4, D_1, D_2 and C_1** A current source is constructed by R_6, R_7, Q_3, and Q_4 which supplies a 600 μA constant current to the UM9151 independent of line power variations. D_2 protects the UM9151 under 5.6V. R_2, the initial power loop, supplies the initial power at the off-hook instant. R_1, the data retention loop, retains the memory during on-hook. **3. Oscillator: CKI, $\overline{CK}$, CK, R_9, R_{10} and C_2** The oscillation frequency is 18 KHz for 10 pps dialing.	BG1: IN4001x4 Q_1: 2N5401 Q_2: 2N5551 Q_3: 2N5401 Q_4: 2N5401 R_1: 22M R_2: 220K R_3: 220K R_4: 220K R_5: 3K3 R_6: 1K R_7: 100K R_8: 220K R_9: 270K R_{10}: 150K C_1: 47μF/10WV C_2: 150pF D_1: 1N4148 D_2: 5V6/0.5W ZD

Test Circuits

(A)



(B)



UMC

UM9151-3

Pulse Dialer

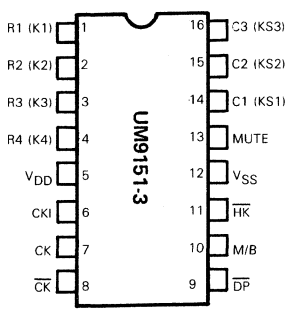
Features

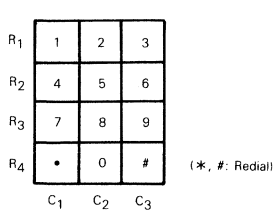
- Direct telephone line operation
- 4 x 3 matrix keyboard interface
- Supply voltage range of 2.0 to 5.5 volts
- Inexpensive RC oscillator
- Low power standby mode for redialing
- 22-digit redial memory
- Redial with either * or # key
- Dialer reset for line power breaks > 200 ms
- 800 ms inter-digit pause
- Selectable make/break ratio
- High speed test capacity

General Description

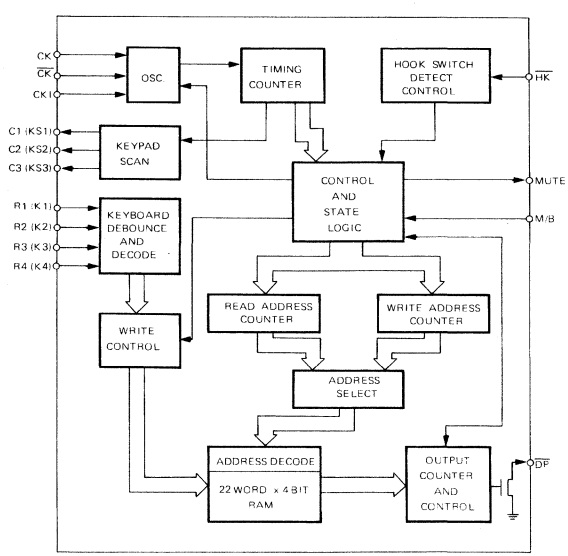
The UM9151-3 pulse dialer is a monolithic CMOS integrated circuit which converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended to replace mechanical telephone dialers and can operate directly from telephone lines. CMOS technology is used to produced this device, resulting in very low power requirements and high noise immunity. The UM9151-3 can be easily interfaced with a variety of telephones, requiring only a minimal number of of external components.

Pin Configuration & Keyboard Assignments





Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage (V_{DD} - V_{SS}) −0.3V to +5.5V
Input Voltage (V_{IN}) ..... −0.3V to V_{DD} + 0.3V
Maximum Power Dissipation (at 25°C) ..... 600 mW
Operating Temperature (Top) ..... −20°C to +70°C
Storage Temperature (T_{STG}) ..... −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

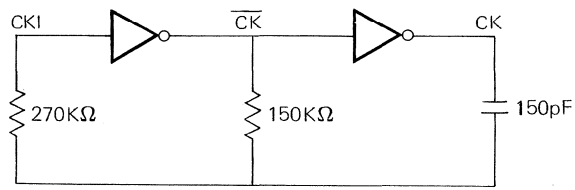
DC Characteristics (V_{DD} = 5.0V, V_{SS} = 0.V, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Tst.Ckt
Operating Voltage	V_{DD}	2.0		5.5	V	off-hook	B
Memory Retention Current	I_{MR}		0.2	1	MA	V_{DD} = 1, $\overline{HS}$ = V_{DD} all outputs unloaded	B
Supply Operating Current	I_{DD}		30	200	μA	oscillator running, all outputs unloaded	B
Standby Current	I_{SD}		0.5	4	μA	$\overline{HS}$ = V_{DD}, all outputs unloaded	A
Output Sink Current Mute $\overline{DP}$	I_{OL}	2	7		mA	V_{DD} = 2.5V, Vo = 0.5V	C
Output Drive Current Mute	I_{OH}	1	6		mA	V_{DD} = 2.5V, Vo = V_{DD}-1V	C
Input Voltage Range	V_{IH}	0.8V_{DD}		V_{DD}	V_{DD}		
	V_{IL}	Vss		0.2Vss			
Keyboard Input Current	I_{KI}	40	60	150	μA	V_{IN} = V_{SS}, all outputs unloaded	

AC Characteristics (V_{DD} = 3.5V, Vss = 0.V, clock freq. = 18KHz or 36KHz, Top = 25°C unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Make/Break Ratio	M/B	M/$\overline{B}$ = V_{DD}			1/2		
		M/$\overline{B}$ = V_{SS}			2/3		
Dial Pulse Rate	DR	Fosc = 18KHz			10		PPS
		Fosc = 36KHz			20		
Make Time	T_M	10PPS	1/2		33		ms
		10PPS	2/3		40		
		20PPS	1/2		16.6		
		20PPS	2/3		20		
Break Time	T_B	10PPS	1/2		66		ms
		10PPS	2/3		60		
		20PPS	1/2		33		
		20PPS	2/3		30		
Inter-digital Pause Time	T_{IDP}	10PPS	1/2		800		ms
		10PPS	2/3		800		
		20PPS	1/2		400		
		20PPS	2/3		400		
Pre-digital Pause	T_{PDP}	10PPS	1/2		800		ms
		10PPS	2/3		800		
		20PPS	1/2		400		
		20PPS	2/3		400		
Mute Delay Time	T_{MDP}	10PPS	1/2		33		ms
		10PPS	2/3		40		
		20PPS	1/2		16.6		
		20PPS	2/3		20		
Key Depression Period	T_{KDP}	V_{IN} = V_{SS} or V_{DD}		30	40		ms
Key Scan Frequency	F_{KS}	C1~C3, R1~R4, Fosc = 18KHz			200		Hz
Clock Frequency	F_{OSC}	R_{CK} I = 270KΩ	V_{DD} = 2.5V	14.3	17.2	18.1	KHz
		$R_{\overline{CK}}$ = 150K,	V_{DD} = 3.9V	17.2	18.0	18.6	
		C_{CK} = 150pF	V_{DD} = 5.0V	17.8	18.2	19.5	

Pin Description

Pin	Designation	Description
1 2 3 4 14 15 16	R1 - R4 C1 - C3	Key inputs. These inputs can be interfaced to either an XY matrix keyboard or a 2 of 7 type keyboard. The keypad inputs are normally held at high. When a key is depressed, scanning signals (typically 200 Hz) are presented at C1, C2, and C3 inputs; the dialer identifies the key by examining the R1 - R4 inputs. Debouncing is provided to avoid false entry.
5 12	V_{DD} V_{SS}	Positive power supply input. Negative power supply input.
6 7 8	CKI,CK,$\overline{CK}$	Oscillator circuit input/output. The oscillator consists of two inverters, with oscillator frequency controlled by external RC components: R_{CKI} = 270K $R_{\overline{CK}}$ = 150K C_{CK} = 150 pF  Oscillator Circuit
9	$\overline{DP}$	Dialing pulse output. This output consists of an N-channel open drain device. Normally this output will be in off state during make and on during break. Dialing pulse rate = 10 PPS and inter-digital pause = 800 ms when Fosc = 18 KHz in normal mode.
10	M/B	Make/Break ratio select input. In normal mode, this input is used to select the Make/Break ratio: when input = V_{DD}, M/B ratio = 1/2 when input = V_{SS}, M/B ratio = 2/3. When connected to the clock output (pin 7), this input can trigger the UM9151-3 into test mode, generating high speed dialing (DPR = 600 PPS, IDP = 13.3 ms).
11	$\overline{HK}$	Hook switch input. This input is used to detect whether the telephone is in the on-hook or off-hook state: V_{DD} = on-hook V_{SS} = off-hook. (Resetting time = 200 ms minimum.)
13	MUTE	Mute output. This output is an inverter normally at low state when there is no key entry. During outdialing it changes to high state and is used to mute the speech network.

Operational Procedures

Symbol Definitions:
Dp: pulse digit (0 through 9)
ZiZiZi: conversation
O-O↑: off-hook.
O-O↓: on-hook.
[*] or [#] : Redial

Recommended Operations:
Normal dialing:
O-O↑; DP...Dp; ZiZiZi; O-O↓.
Dial pulse begins as soon as first key is entered. Debounced and detected on chip.

Redialing:
O-O↑; [*] or [#] key
([*] or [#] key can be accepted as first key entry after off-hook.)

Functional Description

1) N-channel open drain output — $\overline{DP}$ (figure 1).

2) Clock oscillator.
The clock oscillator consists of two inverters, with the frequency of oscillation controlled by external components connected to pins 6, 7, and 8. The circuit is sufficiently versatile to allow the use of a variety of external component configurations. The oscillator circuit is shown in figure 2.

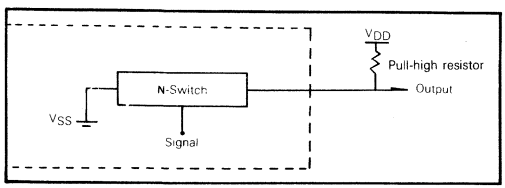


Figure 1

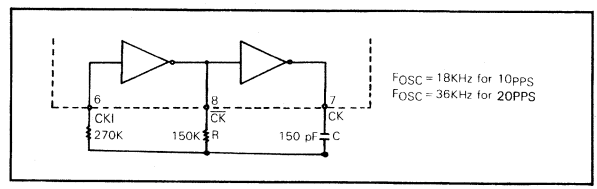
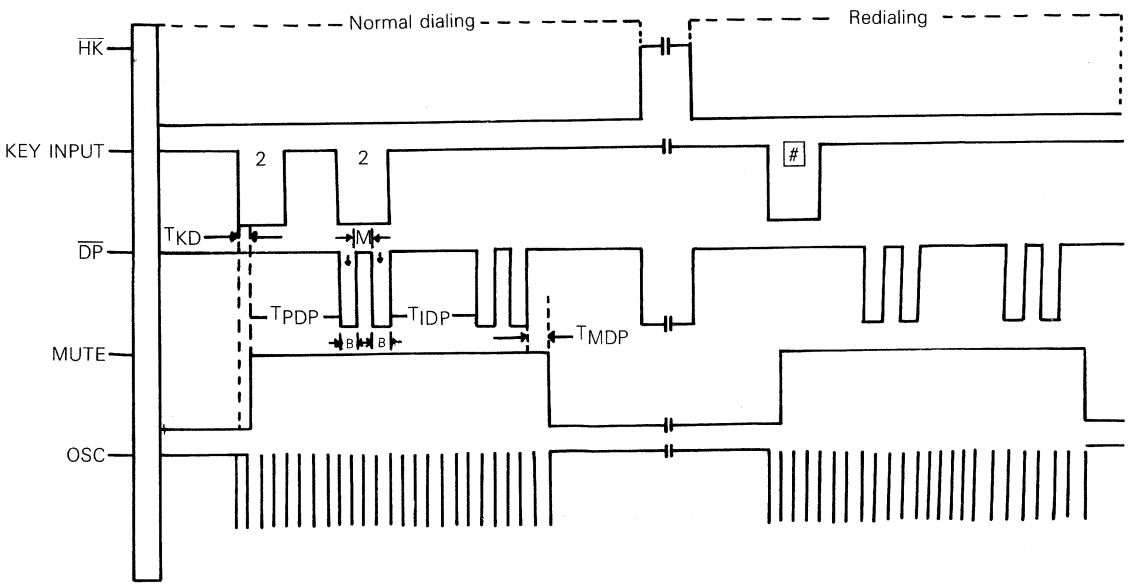


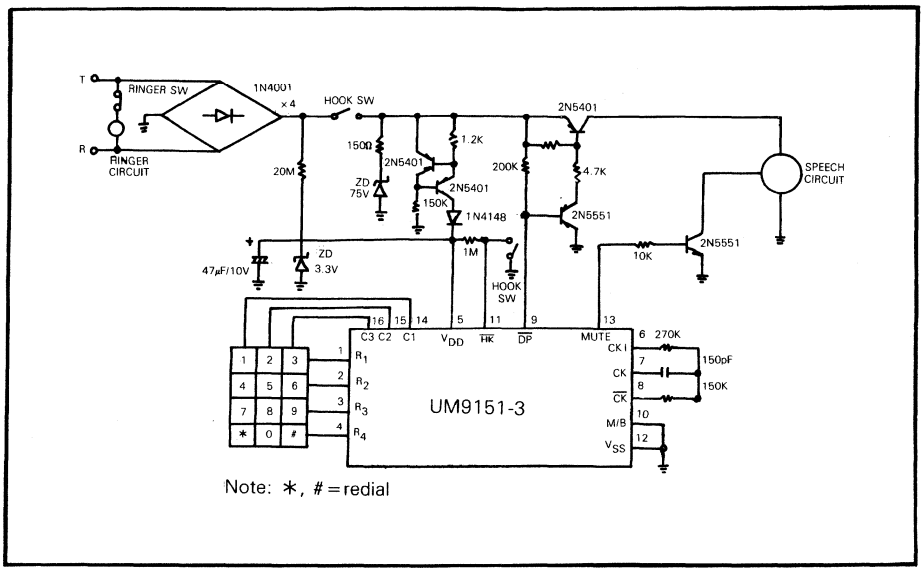
Figure 2.

Timing Diagram



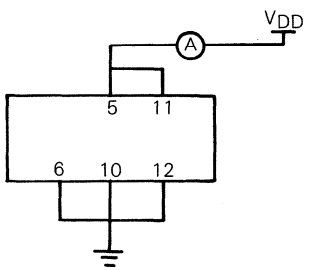
Application Circuit

(M/B = 40/60, IDP = 800ms, DPR = 10PPS, and Fosc = 18KHz in this example.)



Test Circuits

A)



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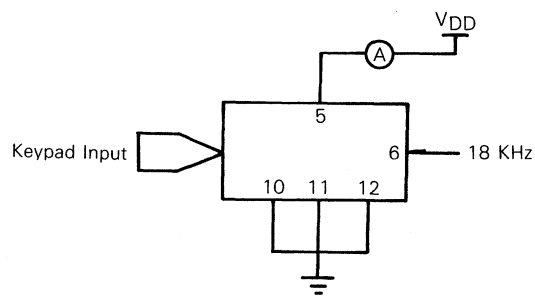
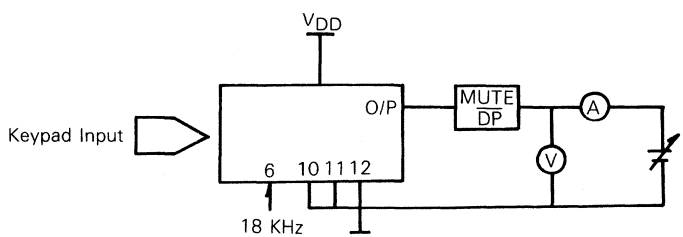


C)



UMC

UM91611

10 Memory Pulse Dialer

Features

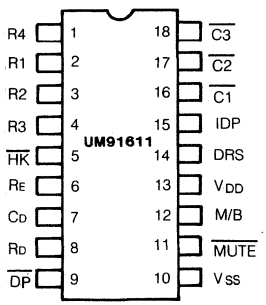
- Ten 18-digit number memories
- 22-digit last number redial memory
- Supply voltage range of 1.5 to 5.0 Volts
- Direct telephone line operation
- Inexpensive RC oscillator design with accuracy better than +/– 5% over temperature and unit to unit variations
- Independent inputs for selecting dialing rate (10 pps/20 pps), make/break ratio (1/2 or 2/3), and inter-digit pause (400 ms/800 ms)
- Can be used with either inexpensive single contact XY matrix keyboard or standard 2 of 7 keyboard
- On-chip mute and pulse drivers
- Call disconnect by pushing [*] and [#] keys simultaneously

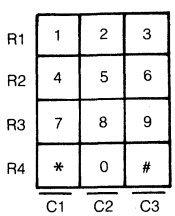
General Description

The UM91611 pulse dialer is a monolithic CMOS integrated circuit which converts pushbutton inputs to a series of pulses suitable for telephone dialing. The UM91611 is pin compatible with the T25610. The UM91611 is an upgraded version of the popular UM9151. In addition to the dialing functions performed by the UM9151, the UM91611 has ten 18-digit number memories and a last-number redial memory with a 22-digit capacity.

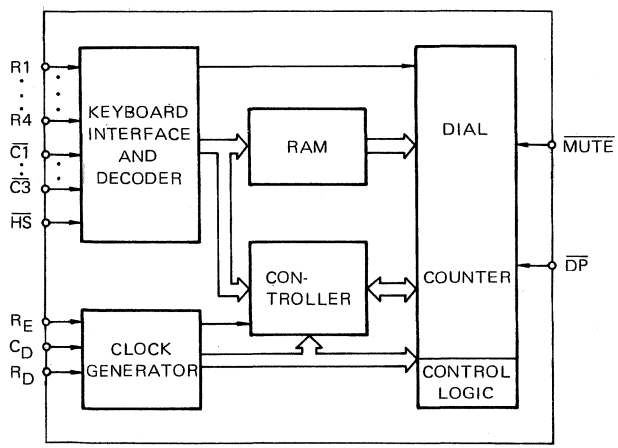
CMOS technology is used to produce this device, resulting in very low power requirements and high noise immunity. The UM91611 can be easily interfaced with a variety of telephones, requiring only a minimum number of external components.

Pin Configuration & Keyboard Assignments





Block Diagram



Absolute Maximum Ratings *

Power supply voltage (V_{DD} -V_{SS}) .....—0.3V to 6.0V
Input voltage (V_{IN}) ..... —0.3V to V_{DD} + 0.3V
Maximum power dissipation (at 25°C) ..... 600 mW
Operating temperature (T_{OP}) ..... —20°C to +70°C
Storage temperature (T_{STG}) ..... —55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, Top = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test CKT
Data Retention Voltage	V_{DR}	1.0			V	ON HOOK ($\overline{HK}$ = V_{DD})	A
Data Retention Current	I_{DR}		0.05	0.15	μA	V_{DD} = 1.0V, $\overline{HK}$ = V_{DD}	A
Operating Voltage	V_{DD}	1.5	2.0	5.5	V		A
Operating Current	I_{DD}			100	μA	V_{DD} = 1.5V, All outputs unloaded	A
				500	μA	V_{DD} = 3.5V, All outputs unloaded	A
$\overline{DP}$ Sink Current	I_{OLDP}	120			μA	V_{DD} = 3.5V, V_{OUT} = 0.4V	B
$\overline{DP}$ Source Current	I_{OHDP}	20			μA	V_{DD} = 1.5V, V_{OUT} = 1.0V	B
		120			μA	V_{DD} = 3.5V, V_{OUT} = 2.5V	B
$\overline{MUTE}$ Sink Current	I_{OLM}	120			μA	V_{DD} = 3.5V, V_{OUT} = 0.4V	B
$\overline{MUTE}$ Source Current	I_{OHM}	20			μA	V_{DD} = 1.5V, V_{OUT} = 1.0V	B
		120			μA	V_{DD} = 3.5V, V_{OUT} = 2.5V	B
Clock Sink Current (R_D Pin)	I_{OLCK}	20			μA	V_{DD} = 1.5V, V_{OUT} = 0.4V	B
Clock Source Current (R_D Pin)	I_{OHCK}	20			μA	V_{DD} = 1.5V, V_{OUT} = 1.0V	B
Input Current High (M/B, DRS, IDP, $\overline{HK}$, R_E)	I_{IH}			0.5	μA	V_{DD} = 3.5V, V_{IN} = 3.5V	C
Input Current Low (M/B, DRS, IDP, $\overline{HK}$, R_E)	I_{IL}			0.5	μA	V_{DD} = 3.5V, V_{IN} = 0.0V	C
Keyboard Input Current	I_{AVE}			60	μA	V_{DD} = 3.5V, One row and one column	—
Input Voltage High	V_{IH}	0.8		1	V_{DD}		—
Input Voltage Low	V_{IL}	0		0.2	V_{DD}		—

AC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, Clock frequency = 2.4KHz Top = 25°C unless otherwise specified)

	Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
PULSE	Make/Break Ratio	M/B	M/B = V_{DD}			1/2		ms
			M/B = V_{SS}			2/3		
	Dial Pulse Rate	DRS	DRS = V_{SS}			10		ms
			DRS = V_{DD}			20		
	Make Time	T_M	10PPS	1/2		33		ms
				2/3		40		
			20PPS	1/2		16.6		
				2/3		20		
	Break Time	T_B	10PPS	1/2		66		ms
				2/3		60		
			20PPS	1/2		33		
				2/3		30		
	Inter-digit Pause Time	T_{IDP}	IDP = V_{DD}			400		ms
			IDP = V_{SS}			800		
	Pre-Digit Pause	T_{PDP}	10PPS	1/2		30		ms
				2/3		37		
			20PPS	1/2		13.6		
				2/3		17		
	Mute Delay Time	T_{MDP}	10PPS	1/2		13.3		ms
				2/3		13.3		
			20PPS	1/2		6.7		
				2/3		6.7		
KEY IN	Keypad debounce time	T_{KD}				13		ms
	Key Scan Frequency	F_{KS}	$\overline{C1}$ ~ $\overline{C3}$, R1 ~ R4, Fosc = 2.4KHz			600		Hz
Oscillator Frequency Fo Stability vs Supply Voltage		$\triangle f_0/f_0$	V_{DD} = 1.5 ~ 3.5V, $R_E = R_D$ = 750Kohm ± 5% C_D = 270pF ± 1%		-10		+10	%
Oscillator Frequency		Fo			1.5		10	KHz
Input Capacitance Any Pin		C_{IN}					10	pF

Pin Description

Pin	Designation	Description
1 2~4 16~18	R4 R1~R3 $\overline{C1}$~$\overline{C3}$	Key inputs. These are the row and column inputs from the keyboard contacts. Active pull-up and pull-down networks are present on these inputs when the device responds to a keyboard entry and starts the oscillator. Debouncing is provided (min. 9 ms) to prevent false entry.
5	$\overline{HK}$	Hook switch input. This input detects the state of the hook switch: $\overline{HK}$ = V_{DD} indicates the on-hook state. $\overline{HK}$ = V_{SS} indicates the off-hook state.
6 7 8	R_E, C_D, R_D	RC oscillator circuit inputs. These pins are provided to connect external resistors R_E and R_D and capacitor C_D to form an RC oscillator that generates the system clock for the UM91611. The oscillator is enabled during the dialing state (pause state included) only. It is disabled at all other times, including the on-hook state. Recommended values for the RC components are $R_E = R_D = 750$Kohm, $C_D = 270$pF, Fo = 2.4 KHz.
9	$\overline{DP}$	Dialing pulse output. This output consists of a CMOS inverter. A sequence of negative going low pulses are available to disconnect from the telephone line.
10 13	V_{SS}, V_{DD}	Power supply inputs. These pins are the power supply inputs: V_{DD} = positive power supply. V_{SS} = negative power supply.
11	$\overline{MUTE}$	Mute output. This output consists of a CMOS inverter that can be used to drive an external bipolar transistor. It is held low during outdialing or on recognition of a key entry and held high at all other times.
12	M/B	Make/break ratio select input. When input on this pin = V_{SS}, the M/B ratio = 1/2. When input = V_{DD}, M/B = 2/3.
14	DRS	Dialing rate select input. When input on this pin = V_{SS}, dialing rate = 10PPS. When input = V_{DD}, dialing rate = 20PPS.
15	IDP	Inter-digit pause select input. When input on this pin = V_{SS}, IDP = 800 ms. When input = V_{DD}, IDP = 400ms.

Operational Procedures

Symbol Definitions
Dp: pulse digit (0 through 9).
Loci: memory location (Loc0-Loc9)
ZiZiZi: conversation.
0-0↑: off-hook.
0-0↓: on-hook.

Recommended Operations

Normal dialing:
0-0↑; Dp...Dp; ZiZiZi; 0-0↓

Dial pulsing begins as soon as the first digit is entered. Pauses may be entered into the dialing sequence by pressing the [#] key (outdialing is not affected.) The total number of digits entered (including the [#] key) should not exceed 22; numbers larger than 22 digits can be dialed out only by waiting for the first 22 digits to be completely dialed out before adding the remaining digits. (For numbers larger than 22 digits the redialing function is inhibited.)

Inhibiting redialing:
0-0↑; Dp.... Dp; *; *.

Dialing must be completed before the * key is pressed. This operation inhibits the redialing function.

Redialing:
0-0↑; Dp...Dp; #; #; 0-0↓.
0-0↑; #; #; ZiZiZi; 0-0↓.

This operation dials out the last number remaining in the buffer memory. Access pause is terminated by pushing the [#] key.

Storing numbers:
0-0↑; *; Dp...Dp; *; Loci; *; Dp...Dp; *; Loci...
Numbers stored may include the [#] key. Storing numbers will not cause any output signal to be sent out.

Transferring last number dialed to memory:
0-0↑; Dp...Dp; *; #; Loci.

After normal dialing has been completed, this procedure can be used to store the last number dialed to memory.

Repertory dialing from number memories:
0-0↑; #; Loci ...; #; Loci...

In repertory dialing, the first memory number must be completely dialed out before the next [#] key entry. If a number dialed out from memory contains a pause([#] key entry), manual depause (by pressing the [#] key) is necessary to terminate the pause state before outdialing will resume.

Normal dialing after repertory dialing or redialing:
0-0↑; #; #; or #; Loci; ... (when dialing is completed) Dp...Dp.

Clearing number memory locations:

0-0↑; *; #; *; Loci...
This operation clears the number stored in memory location i. It is equivalent to storing a pause as the first digit in memory.

Call disconnect:
0-0↑;....* #

Pressing the [*] and [#] keys simultaneously forces the $\overline{DP}$ output to low, thus disconnecting the current dialing sequence.

Functional Description

Keyboard Definitions

	$\overline{C1}$	$\overline{C2}$	$\overline{C3}$
R1	1	2	3
R2	4	5	6
R3	7	8	9
R4		0	#

Digits 0 through 9 function as dial numbers in normal dialing mode and number storing mode, and represent memory locations when entered after the [#] (for redial) or [*] (for number storing mode) keys.

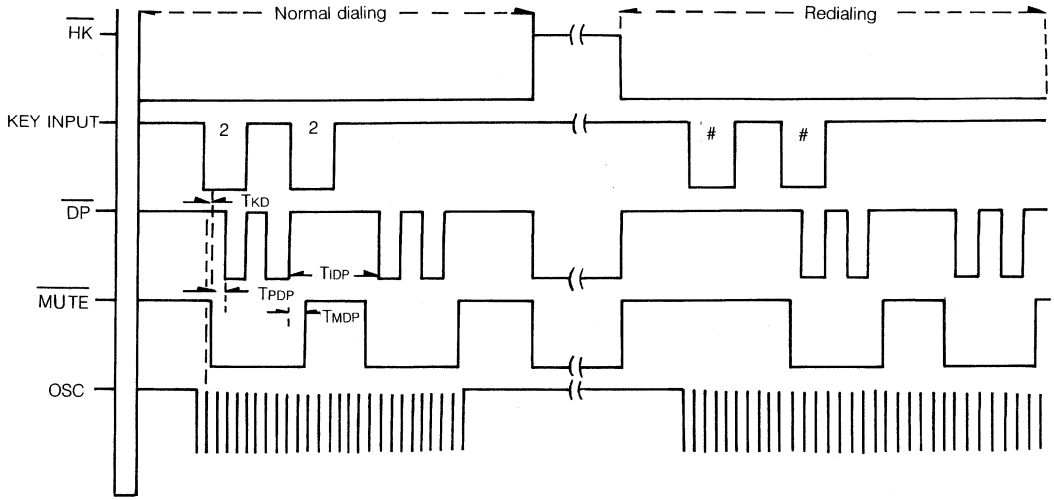
The [*] key functions as the initial and final step in the number storing operation. It also represents a state change in inhibit redialing, last number dialed transfer, and call disconnect operations.

The [#] key initiates redialing or repertory memory dialing. It also represents the number stored in the redial buffer memory when pressed second during the redialing operation. In normal dialing and number storing, [#] represents a pause in the dialing sequence; when a pause is met in outdialing, pressing [#] again functions as a depause.

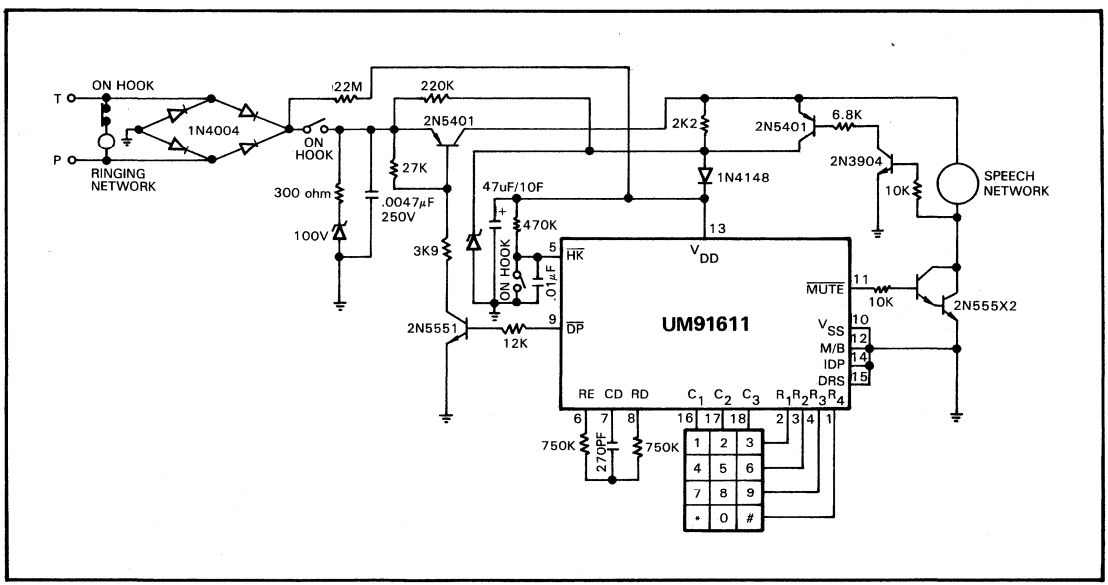
When the [#] and [*] keys are pressed simultaneously a call disconnect operation takes place. Lastly, when transferring the last number dialed to memory, the [#] key, when pressed after the [*] key, represents the last number dialed.

Dialing Pulse Output Structure
The UM91611 has a make first and break next structure. When the first digit in RAM is dialed out a logic circuit checks immediately to see if the following digit is waiting to be dialed out. If the following digit is ready to be dialed out an interdigit pause is delayed; otherwise the oscillator will be disabled immediately. The UM91611 essentially uses a post-digit pause to meet the EIA RS-470 inter-digit pause requirement.

Timing Diagram

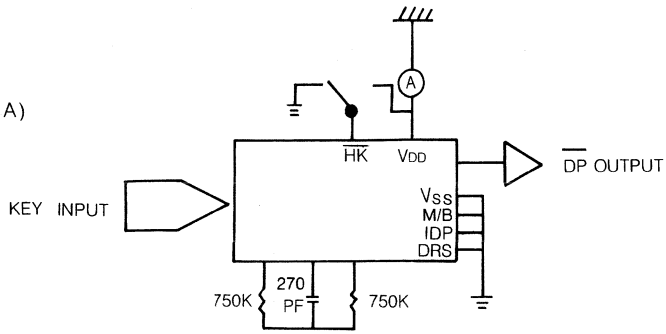


Application Circuit



Test Circuits

(A)



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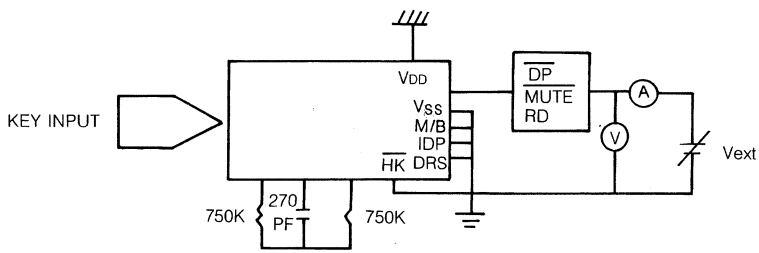
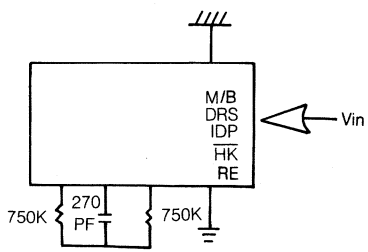


(C)



Tone/Pulse Dialer

Part No.	Description	Page
UM91210/30	Tone/Pulse Dialer	2-3
UM91214/15 Series	Tone/Pulse Dialer	2-17
UM91260/61	10 Memory Tone/Pulse Dialer	2-30
UM91265	Tone/Pulse Dialer	2-41
UM91270	20 Memory Tone/Pulse Dialer	2-53
UM91271/72	20 Memory Tone/Pulse Dialer	2-64
UM91310 Series	Tone/Pulse Dialer	2-76

UMC

UM91210/30

Tone/Pulse Dialer

Features

- 32-digit Redial Memory
- Tone/Pulse Switchable via slide switch
- Wide operating voltage: 2.0V to 5.5V
- Uses inexpensive 3.58 MHz TV crystal
- Pin selectable Make/Break ratio (1/2 or 2/3)
- Key-in tone output for valid key entry in Pulse mode (91230 C/D only)
- 630 millisecond flash time
- "T" key controlled switching from Pulse to Tone mode (91230 C/D only)
- 18-pin or 22-pin DIP
- With minimum tone duration 110 ms

General Description

The products in this series are Tone/Pulse switchable dialers with 32-digit redial memory. Switching from Pulse to DTMF mode can be accomplished either by using a slide switch or by depressing the [T] key.

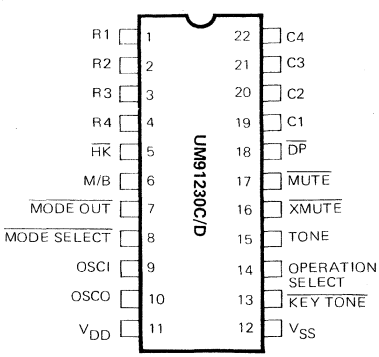
The necessary dual-tone frequencies are all derived from a 3.58 MHz TV crystal, thus providing high accuracy and stability. The sinusoidal waveform for each individual tone is digitally synthesized on the chip. Waveforms thus generated have low total harmonic distortion (5% max.). A reference voltage is generated on the chip which is stable over the operating voltage and temperature range. It regulates the signal levels of the dual tones to meet telephone industry specifications.

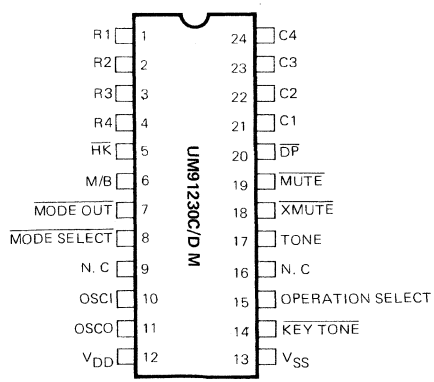
CMOS technology is used in the production of these devices, resulting in low power requirements and high noise immunity. These devices can be easily interfaced with a variety of telephones, requiring only a minimum number of external components.

Ordering Information

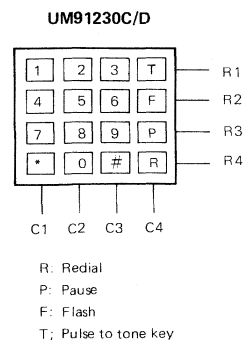
Part Number	Dialing Rate	Package
UM91210C/10CM	10 pps	P-DIP 18L/SO 20L
UM91210D/10DM	20 pps	P-DIP 18L/SO 20L
UM91230C/30CM	10 pps	P-DIP 22L/SO 24L
UM91230D/30DM	20 pps	P-DIP 22L/SO 24L

Pin Configurations

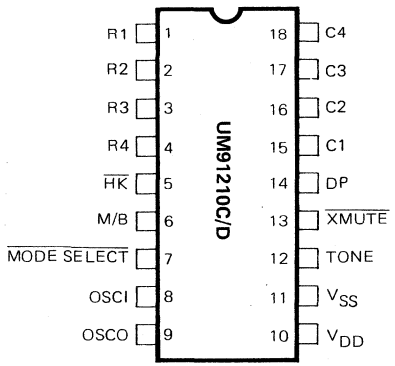


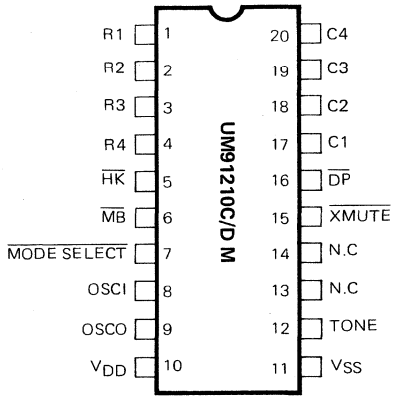


Keyboard Assignments

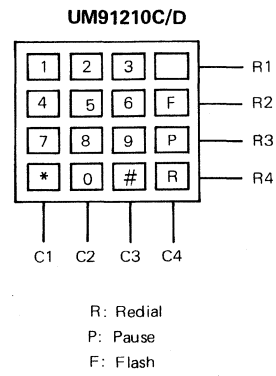


Pin Configurations (Continued)

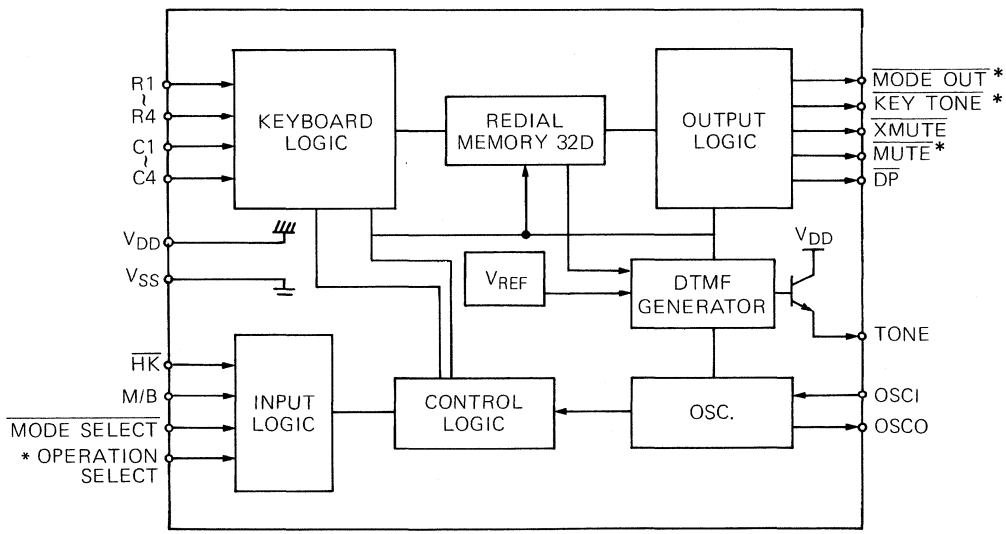




Keyboard Assignments (Continued)



Block Diagram



* : Bonding Option

Absolute Maximum Ratings*

Power Supply Voltage..... −0.3V to +0.6V
Input Voltage..... −0.3V to V_{DD}+0.3V
Maximum Power Dissipation (at 25°C).....500mW
Operating Temperature (T_{OP})..... −20°C to 70°C
Storage Temperature (T_{STG})..... −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 3.579MHz and T_{OP} = 25°C unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD}	2.0		5.5	V	Pulse mode	A
		2.0		5.5	V		
Memory Retention Voltage	V_{MR}	1.0			V		
Memory Retention Current	I_{MR}		0.05	0.05	μA	V_{DD}=1.0V $\overline{HK}$ = V_{DD} All outputs unloaded	
Supply Operating Current	I_{DOP}		0.43	1	mA	Pulse Mode | Oscillator running.	A
	I_{DOT}		0.70	2	mA	DTMF Mode | All outputs unloaded	
Standby Current	I_{SD}		15	50	μA	V_{DD}=2.5V $\overline{HK}$ = V_{SS} All outputs unloaded	A
Output Sink Current $\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$	I_{OL1}	1.7	5.0		mA	V_{OL}=0.4V	B
	I_{OL2}	0.5	1.5		mA	V_{OL}=0.4V V_{DD}=2.0V	
Input Voltage Range	V_{IH}	0.8		1	V_{DD}		
	V_{IL}	0		0.2	V_{DD}		
Row Input Current	I_R		10		μA	V_{IN}=0V | All outputs	C
Col. Input Current	I_C		10		μA	V_{IN}=0V | unloaded	C
Single Column Tone Output Amplitude	V_{OC}	640	700	760	mVp-p	R_{LOAD}=10KΩ, V_{DD}=2.5V	D
		640	700	760		R_{LOAD}=10KΩ, V_{DD}=5.5V	D
Single Row Tone Output Amplitude	V_{OR}	510	560	610	mVp-p	R_{LOAD}=10KΩ, V_{DD}=2.5V	D
		510	560	610		R_{LOAD}=10KΩ, V_{DD}=5.5V	D
Pre-emphasis	Twist	1.7	2	2.3	dB		D
Valley of Single Tone	V_V		V_{DD}-1.8	V_{DD}-1.6	V_{DD}	V_{DD}=3.5V	D
Distortion	DIS		1	5	%	* Note 1	D

* Note 1: $DIS(\%) = \frac{100(V_1^2 + V_2^2 ..... Vn^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$

1. V_1...Vn are the intermodulation or harmonic frequencies in the 500 Hz to 3400 Hz band.
2. V_{IH} and V_{IL} are the individual frequency components of the DTMF signal.

AC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 3.579545 MHz and T_{OP} = 25°C unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
PULSE							
Make/Break Ratio	M/B	M/B = V_{DD}			1/2		%
		M/B = V_{SS}			2/3		
Dial Pulse Rate	DR	UM91210C/UM91230C			9.7		pps
		UM91210D/UM91230D			19.4		
Make Time	T_M	10 pps	M/B=1/2		33.3		ms
			M/B=2/3		40.0		
		20 pps	M/B=1/2		16.7		
			M/B=2/3		20.0		
Break Time	T_B	10 pps	M/B=1/2		66.7		ms
			M/B=2/3		60		
		20 pps	M/B=1/2		33.3		
			M/B=2/3		30		
Interdigit Pause Time	T_{IDP}	10 pps	M/B=1/2		876		ms
			M/B=2/3		870		
		20 pps	M/B=1/2		893		
			M/B=2/3		890		
Predigit Pause	T_{PDP}	10 pps	M/B=1/2		19.5		ms
			M/B=2/3		19.5		
		20 pps	M/B=1/2		19.5		
			M/B=2/3		19.5		
$\overline{\text{XMUTE}}$ $\overline{\text{MUTE}}$ Delay Time	T_{MDP}	10 pps	M/B=1/2		850		ms
			M/B=2/3		850		
		20 pps	M/B=1/2		850		
			M/B=2/3		850		
TONE							
Minimum Tone Duration	T_{MFD}				110		ms
Minimum Tone Interdigit Pause	T_{TIDP}				110		ms
Tone Output Predigit Pause	T_{TPDP}				0		ms
$\overline{\text{XMUTE}}$ Delay Time	T_{MDT}				110		ms
Auto Pause Time	T_{AP}				3.6		s
Flash Time	T_F				630		ms
Oscillator Startup Time	T_{START}				10		ms
$\overline{\text{XMUTE}}$, $\overline{\text{MUTE}}$ Startup Time	T_{MS}				15		ms

AC Characteristics (Continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
KEY-IN						
Keypad Debounce Time	T_{KD}			23		ms
Key Scan Frequency	F_{KS}			445		Hz
KEY-IN TONE						
Key-in Tone Duration Time	T_{KTD}			23		ms
Key-in Tone Frequency	F_{KT}			18		KHz
Key-in Tone Startup Time	$T_{KTSTART}$			15		ms

Row/Column	Condition	Spec.	Actual	Error(%)	Unit
R1	F_{OSC} = 3.579MHz	697	699.1	+0.31	Hz
R2		770	766.2	−0.49	Hz
R3		852	847.4	−0.54	Hz
R4		941	948.0	+0.74	Hz
C1		1,209	1,215.9	+0.57	Hz
C2		1,336	1,331.7	−0.32	Hz
C3		1,477	1,471.9	−0.35	Hz

Pin Description

Pin		Designation	Description
91210	91230		
1	1	R1	Input Keys.
2	2	R2	These pins serve as an interface to an XY matrix keyboard. C1 through C4 and
3	3	R3	R1 through R4 are set to low at On Hook ($\overline{HK}$=high). C1 through C4 are set to
4	4	R4	low and R1 through R4 are set to high at Off Hook ($\overline{HK}$=low), which enables
15	19	C1	the key-in operation.
16	20	C2	The Oscillator starts running when a keypress is detected. Scanning signals are
17	21	C3	presented at both column and row input signals (Typ: 445 Hz) until the input
18	22	C4	key is released. Key-in is compatible with standard 2-of-8 form or single-contact keyboards. Debouncing is provided to avoid false entry (Typ.: 23 ms).
5	5	$\overline{HK}$	Hook Switch Input . This input detects the state of the hook switch contact. $\overline{HK}$ = V_{DD}: On-hook, chip unactivated $\overline{HK}$ = V_{SS}: Off-hook, chip active
6	6	M/B	Make/Break Ratio Select Input. This input allows selection of the Make/Break ratio (33.3:66.7/40:60) M/B = V_{DD}: 33.3/66.6 M/B = V_{SS}: 40/60

Pin Description (Continued)

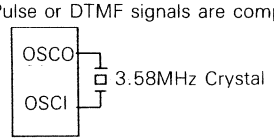
<table>
<tr><th colspan="2">Pin</th><th rowspan="2">Designation</th><th rowspan="2">Description</th></tr>
<tr><th>91210</th><th>91230</th></tr>
<tr><td></td><td>7</td><td>$\overline{\text{MODE OUT}}$</td><td>Mode Output.
This output indicates whether the chip is operating in Pulse or Tone mode. Pulse/Tone modes correspond to the OFF/ON states (N-channel open drain). Mode state is controlled by the Operation Select, $\overline{\text{MODE SELECT}}$, and [T] key inputs.</td></tr>
<tr><td>7</td><td>8</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input.
This input allows the selection of Pulse mode or DTMF mode.
$\overline{\text{MODE SELECT}}$ = V_{DD}: pulse mode operation
$\overline{\text{MODE SELECT}}$ = V_{SS}: tone mode operation</td></tr>
<tr><td>8
9</td><td>9
10</td><td>O_{SCI}
O_{SCO}</td><td>Oscillator Input/Output.
These pins connect an external 3.58 MHz crystal to the UM91210/UM91230. Oscillation starts when the chip encounters the Off-Hook condition and is sustained until all Pulse or DTMF signals are completed.
  </td></tr>
<tr><td>10
11</td><td>11
12</td><td>V_{DD}
V_{SS}</td><td>Power.
These pins are the positive and negative power supply inputs.
This device is designed to operate at 2.0V to 5.5V.</td></tr>
<tr><td></td><td>13</td><td>$\overline{\text{KEY TONE}}$</td><td>Key-in Tone Output.
The key-in tone signal is provided for all key entries in the Pulse mode, except for the [T] key. No $\overline{\text{KEY TONE}}$ signal is generated in the DTMF mode. F_{KT}: 1.8 KHz, T_{KT}: 23 ms, (N-channel open drain).</td></tr>
<tr><td></td><td>14</td><td>OPERATION SELECT</td><td>Operation Select Input.
The operating mode can be switched from Pulse to DTMF by this input, whether the entry is made by the [T] key or by the $\overline{\text{MODE SELECT}}$ input. (See Table 8-1)

Table 8-1
<table>
<tr><th>Operation Select</th><th>$\overline{\text{MODE SELECT}}$</th><th>Initial Mode</th><th>Switching Entry Mode</th><th>Notes</th></tr>
<tr><td rowspan="2">V_{DD}</td><td>V_{DD}</td><td>Pulse</td><td>[T] key-in</td><td rowspan="2">$\overline{\text{MODE SELECT}}$ defines only initial mode after going Off Hook and is latched at first key entry.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
<tr><td rowspan="2">V_{SS}</td><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ Input = V_{SS}</td><td rowspan="2">[T] key is disabled under this condition.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>12</td><td>15</td><td>TONE</td><td>DTMF Signal (Output)
When a valid keypress is detected in DTMF mode, appropriate low group and high group frequencies are generated which hybridize the Dual Tone output. Tone out is in the Off state in pulse mode.</td></tr>
</table>

Pin Description (Continued)

Pin		Designation	Description
91210	91230		
13	16	$\overline{XMUTE}$	Xmute (Output) N-channel open drain. $\overline{HK}$ = V_{DD}: XMUTE OUTPUT = OFF $\overline{HK}$ = V_{SS}: Normally Off On during Pulse and DTMF dialing.
	17	$\overline{MUTE}$	Mute (Output) N-channel open drain. $\overline{HK}$ = V_{DD}: MUTE OUTPUT = OFF $\overline{HK}$ = V_{SS}: Normally Off in DTMF mode. On during Pulse dialing.
14	18	$\overline{DP}$	Dial Pulse (Output) This output will normally be OFF during Break and ON during make at Off-Hook ($\overline{HK}$ = V_{SS}). The output will be ON at On-Hook. (N-channel open drain).

Operation Procedures

Symbol definitions

Dp: Pulse digit, 1,2,3,4,5,6,7,8,9,0.
Dt: Tone digit, 1,2,3,4,5,6,7,8,9,0,*,#.
ZiZiZi: Conversation.
0-0↑: Off-hook.
0-0↓: On-hook.
⌐: Input level from low to high
¬: Input level from high to low.

Recommended Dialing, Redialing, Mixed Dialing operations

1. Normal Dialing in Pulse Mode
   0-0↑, Dp.....Dp, ZiZiZi, 0-0↓.

2. Normal Dialing in Tone Mode
   a. 0-0↑, Dt.....Dt, ZiZiZi, 0-0↓.
   b. 0-0↑, T, Dt.....Dt, ZiZiZi, 0-0↓. (UM91230C/D only)

3. Manual Dialing with Automatic Access Pause
   a. 0-0↑, Dp, P, Dp.....Dp, ZiZiZi, 0-0↓ or
   b. 0-0↑, Dt, P, Dt.....Dt, ZiZiZi, 0-0↓.

   Note: Each [P] key-in provides 3.6 seconds of pause time. [P] key entry is ignored if it is the first digit after going Off Hook. The [*] key can also be used as a pause key in pulse mode. A pause can be cancelled with the [P], [T] or [R] keys during pause time when redialing.

4. Redialing
   a. 0-0↑, Dp.....Dp, 0-0↓, 0-0↑, [R].
   b. 0-0↑, Dt.....Dt, 0-0↓, 0-0↑, [R].

   Note: The [R] key is disabled while Pulse or DTMF signals are being transmitted. When more than 32 digits have been dialed as a single number, redialing will be inhibited. The [#] key can be used as an [R] key in Pulse mode.

5. Inhibiting Redial
   a. 0-0↑, Dp.....Dp, [R], [R].
   b. 0-0↑, Dt.....Dt, [R], [R].

   Note: Lift the receiver. Dial a number in Pulse mode. Press the [R] key twice.

6. Pulse/Tone Switchable Operations
   a. Mode switching by $\overline{MODE\ SELECT}$ input: (For UM91230C/D, OPERATION SELECT = V_{SS}.)
   0-0↑, Dp.....Dp, P, $\overline{MODE\ SELECT}$, ¬, Dt..... Dt
   ⊢——Pulse mode——⊣Tone Mode

Tone/Pulse Dialer

Note: If the [P] key is not pressed as one of the series of digits before or after the mode is switched, the following condition will result:
(1) If a Tone digit is pressed after the Pulse digits have finished going out, the DTMF mode will be implemented after the last Pulse signal has been transmitted in this mode. Tone digits will be transmitted from the Tone Out pin as a DTMF signal when the corresponding keys are depressed.

(2) If Tone digits are keyed in while the Pulse signal is still being sent out, the DTMF mode will take over but will be put on hold until the last Pulse signal has gone out. MODE OUT will flash to indicate that you are now in the hold state (for UM91230C/D only). Tone digits will be stored in Redial memory as DTMF data, but will not be transmitted from TONE OUT. When the data is ready for transmission from Redial Memory, the [T] (for UM91230C/D only), [R] or [P] keys can be pressed to reset the Hold state and the DTMF data will be serially transmitted.

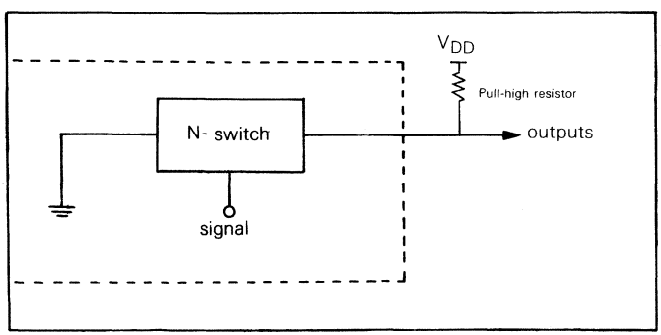
b. Mode Switching by [T] key: (OPERATION SELECT = V_{DD} for UM91230C/D only)
0-01, Dp,.....Dp, P, T, Dt.....Dt
|—Pulse mode —|Tone mode|

Note: If the [P] key is not pressed serially before or after the [T] key, the following conditions will result:
(1) If a Tone digit is pressed after the digits in the Pulse mode have finished going out, the DTMF mode will become operational after transmission of the last Pulse signal. In this mode, the Tone digits are transmitted from TONE OUT as DTMF signals when the corresponding keys are depressed.
(2) If a Tone digit is pressed while the Pulse signals are still going out, the DTMF mode will become operational but will remain in the Pause state after the last Pulse signal has been transmitted. $\overline{\text{MODE OUT}}$ will flash to indicate that you are in the Pause state and the remaining Tone digits will be stored in redial memory as DTMF data but will not be transmitted from Tone Out. When the chip is ready to transmit the DTMF data in Redial Memory, the [T], [R], or [P] keys can be depressed to reset the Pause state and the DTMF data will be serially transmitted.

7. Redial with the Pause State Cancelled
0-01, [R], [P], or [T].
Note: (1) Pause time can be cancelled by pressing the [P], [R] or [T] keys during pause time when redialing. Any other pause in the series is also cancelled.
(2) If a pause was not stored before or after the mode was switched, the chip will go into the Pause state when the DTMF mode is activated. $\overline{\text{MODE OUT}}$ will flash to indicate that you are in the Pause state. DTMF data will be stored in the Redial Memory and not transmitted from Tone Out. After [R], [P] or [T] are depressed to reset the Pause state, DTMF data will be serially transmitted.

Functional Description

1. N-Channel Open Drain Output:
$\overline{\text{DP}}$, $\overline{\text{MUTE}}$, $\overline{\text{XMUTE}}$, $\overline{\text{MODE OUT}}$, $\overline{\text{KEY TONE}}$



2. DTMF Generation

The DTMF signal is produced from the Tone Frequency Generator circuit with an NPN transistor-emitter-follower output buffer (Figure 1, below). The digitally synthesized sine wave is well designed, with an eight-level, 16-segment, fixed amplitude. It provides (V_{DD}-1.8V) a reference voltage structure (Figure 2). The Total Harmonic Distortion (THD) of the DTMF output is 5% maximum. THD versus Operating Voltage and DTMF output amplitude versus Operating Voltage is shown in Figure 3 and Figure 4.

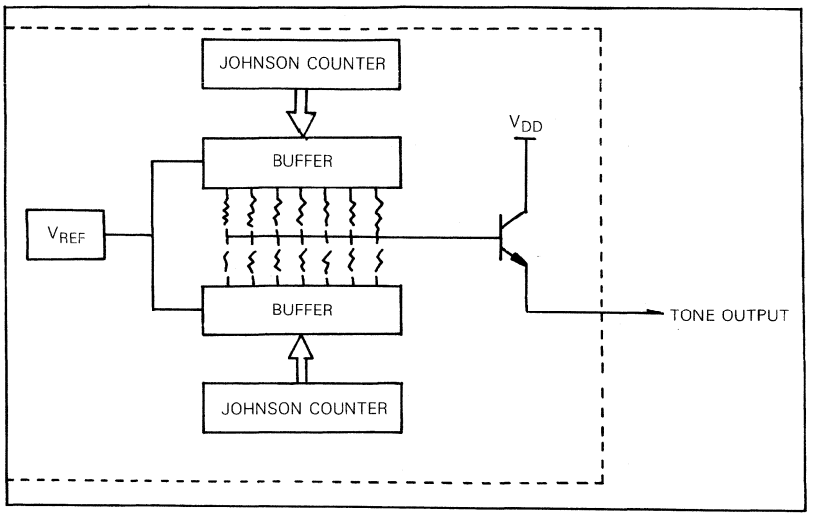


Figure 1.

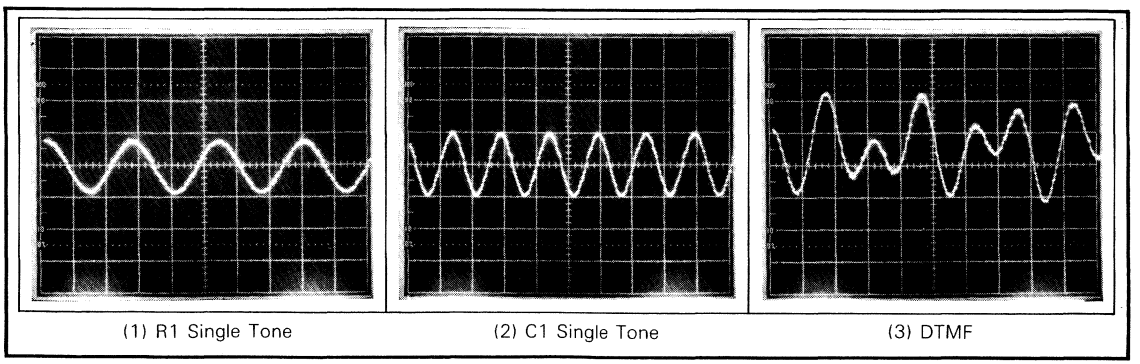


Figure 2: Waveforms

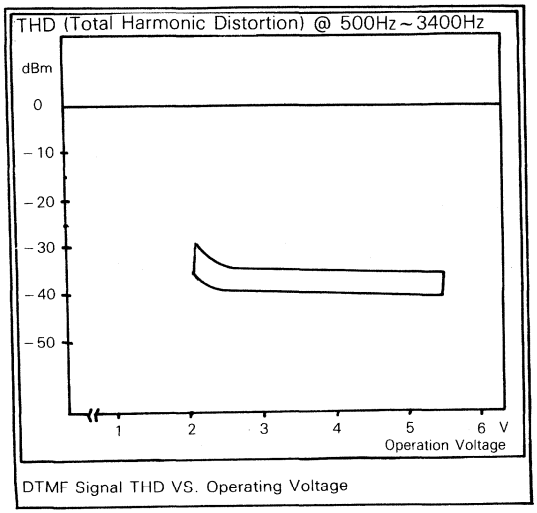


Figure 3

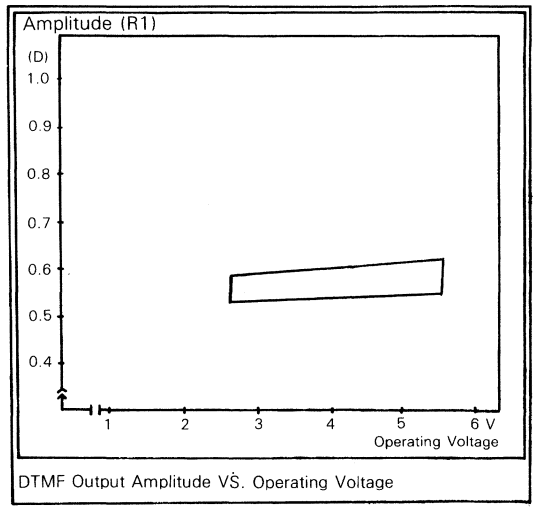


Figure 4

3. Single Tone Operation in DTMF Mode (Test Mode)
   The [*] and [#] keys are used to trigger the chip into test mode by depressing them simultaneously during Off-Hook.

   The single tone keyboard assignments are shown in the following table in contrast with normal mode.

Normal mode

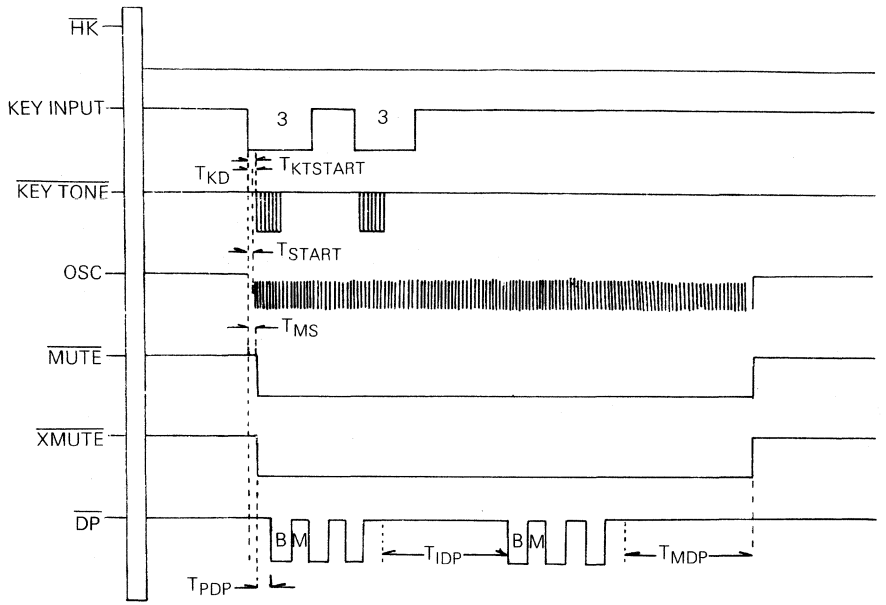
	C_1	C_2	C_3
R_1	1	2	3
R_2	4	5	6
R_3	7	8	9
R_4	*	0	#

Single tone mode

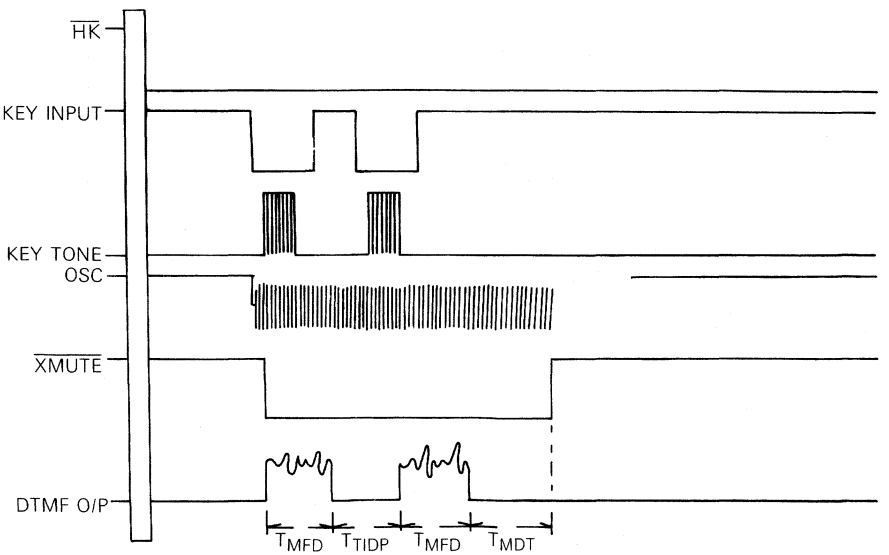
	C_1	C_2	C_3
R_1	R_1	C_2	C_3
R_2	C_1	C_2	R_2
R_3	R_3	C_2	C_3
R_4	C_1	R_4	C_3

Timing Diagrams

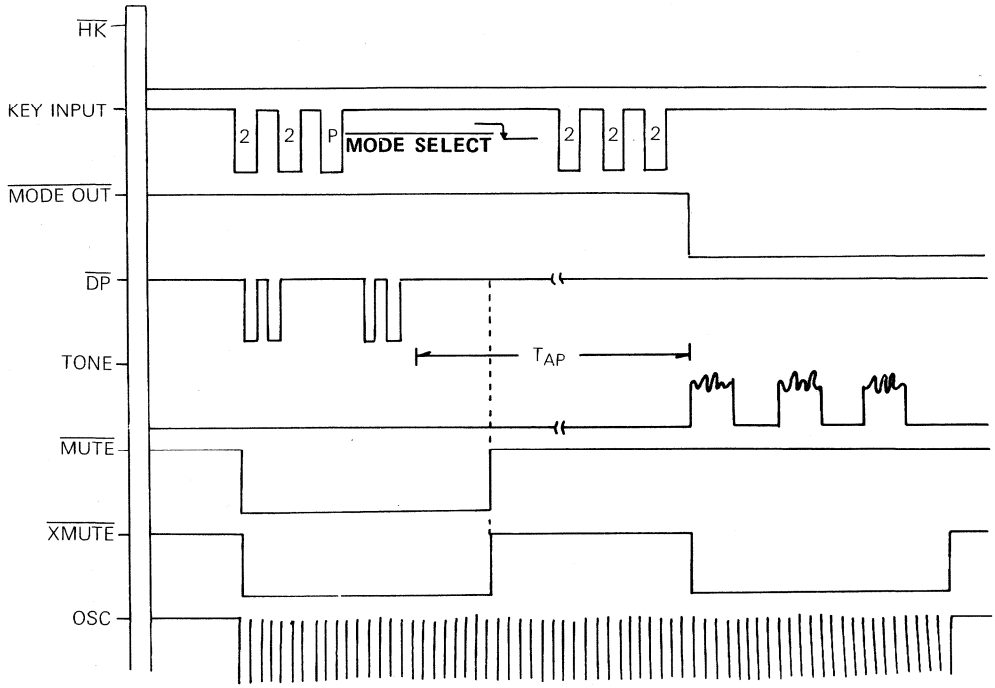
1. PULSE MODE TIMING DIAGRAM



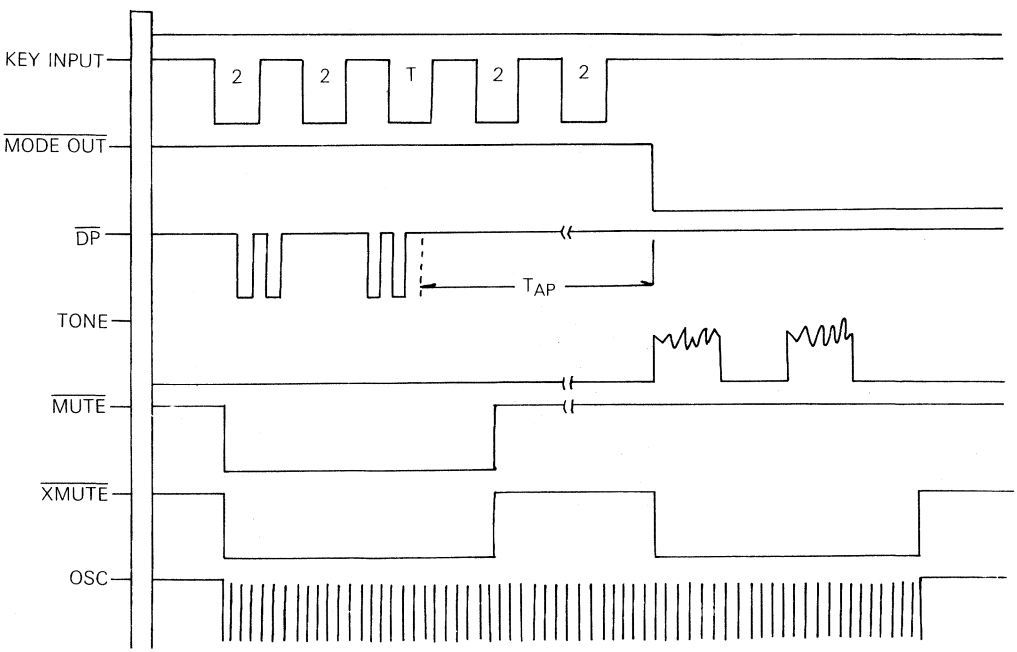
2. TONE MODE TIMING DIAGRAM



3. NORMAL PULSE to TONE MIXED DIALING VIA MODE SELECT SLIDE SWITCH (OPERATION SELECT = V_{SS} for UM91230C/D)



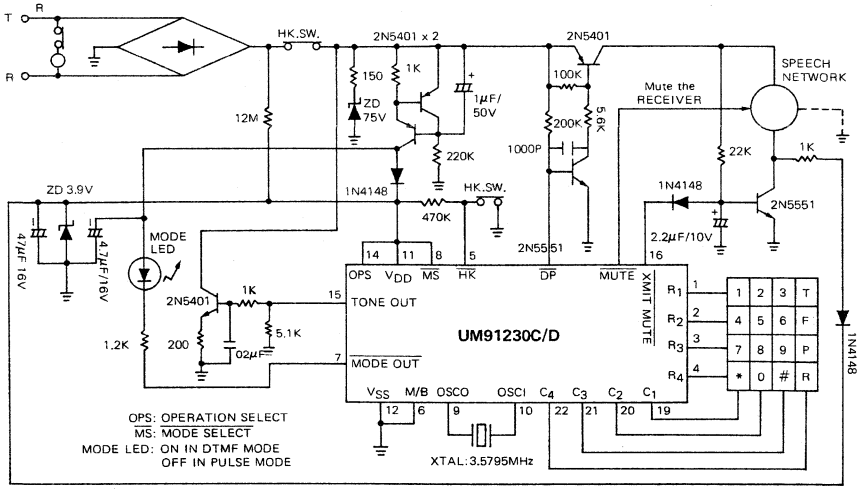
4. NORMAL PULSE to TONE MIXED DIALING VIA [T] KEY (OPERATION SELECT = V_{DD} THIS OPERATION for UM91230C/D ONLY.)



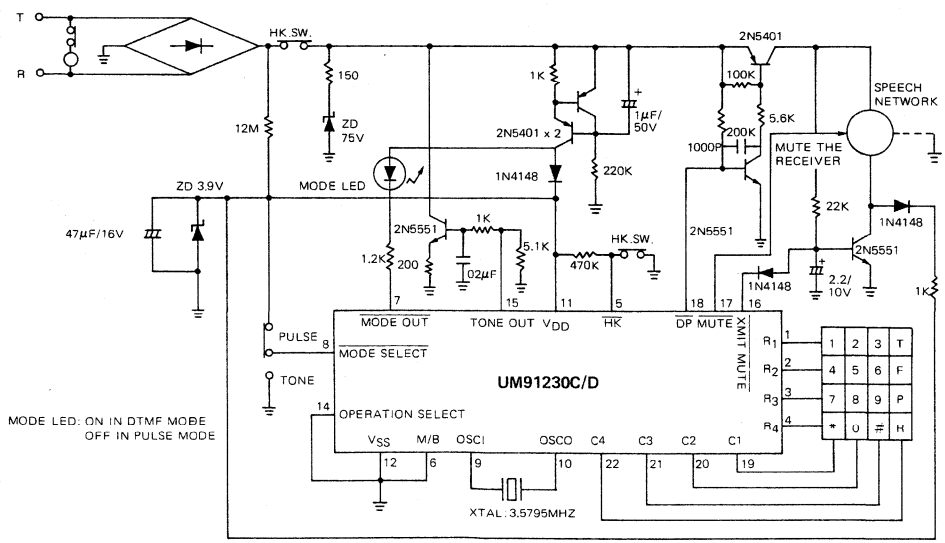
Application Circuits

1. UM91230C/D

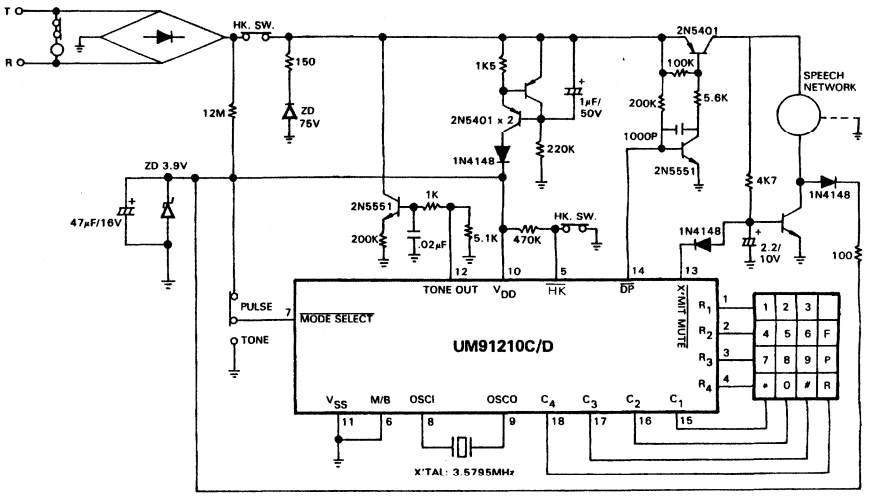
1) Switching mode by [T] key ($\overline{\text{MODE SELECT}}$, OPERATION SELECT = V_{DD})



2) Switching mode by $\overline{\text{MODE SELECT}}$ (OPERATION SELECT = V_{SS})

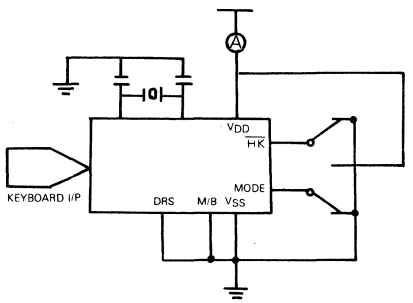


2. UM91210C/D

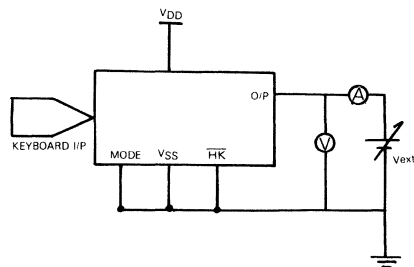


Test Circuits

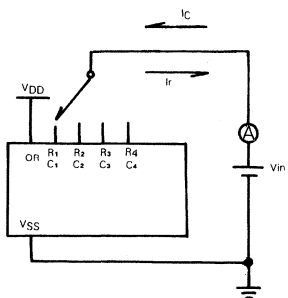
(A)



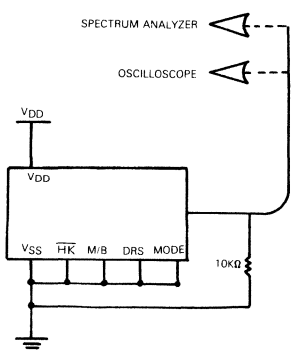
(B)



(C)



(D)



- OSCILLOSCOPE: TEKTRONIX 468
- SPECTRUM ANALYZER: HP 3585A

UMC

UM91214/15 Series

Tone/Pulse Dialer

Features

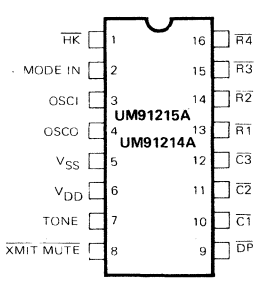
- One touch redial operation
- Tone/Pulse switchable
- 32-digit capacity for redialing
- Automatic mixed redialing (last number redial) of pulse to DTMF with multiple automatic access pauses.
- PABX auto-pause is 2.2 seconds
- DTMF Timing:
  Manual dialing: minimum duration for bursts and pauses
  Redialing: calibrated timing
- Hands-free control function
- Wide operating voltage range: 2V to 5.5V
- Key-in beep tone output
- Digits dialed manually after redialing are cascadable and stored as additional digits for the next redialing
- Uses inexpensive ceramic resonator (3.58 MHz)
- Two versions for different telephone systems
- Built-in power up reset circuit
- Four extra function keys: flash, pause, redial and DP or DTMF mixed dialing
- Four-by-four (or 2 of 8) keyboard can be used
- Low standby current

General Description

The UM91214/15 is a single-chip, silicon gate, CMOS integrated circuit with an on-chip oscillator for a 3.58 MHz crystal or ceramic resonator. It provides dialing pulse (DP) or dual tone multi-frequency (DTMF) dialing. A standard 4 x 4 matrix keyboard can be used to support either DP or DTMF modes. Up to 32 digits can be saved in the on-chip RAM for redialing. In the DTMF mode, minimum tone duration and minimum intertone pause provide for rapid dialing. Maximum tone duration is dependent upon the key depression time in manual dialing.

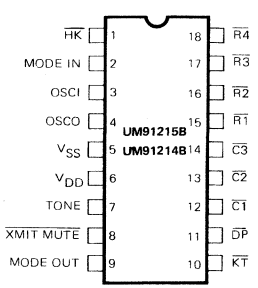
Pin Configurations

a. 16 Pin Package

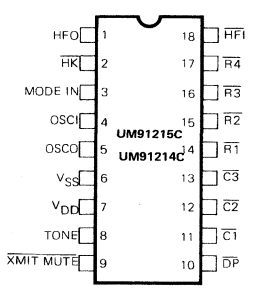


b. 18 Pin Packages

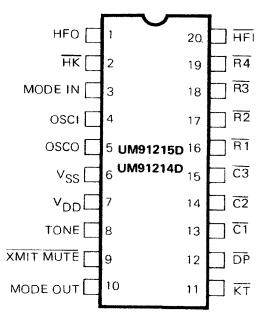
(i) Key tone output



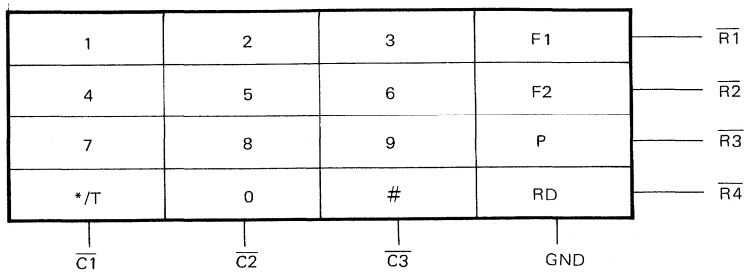
(ii) Hands free control



c. 20 Pin Package

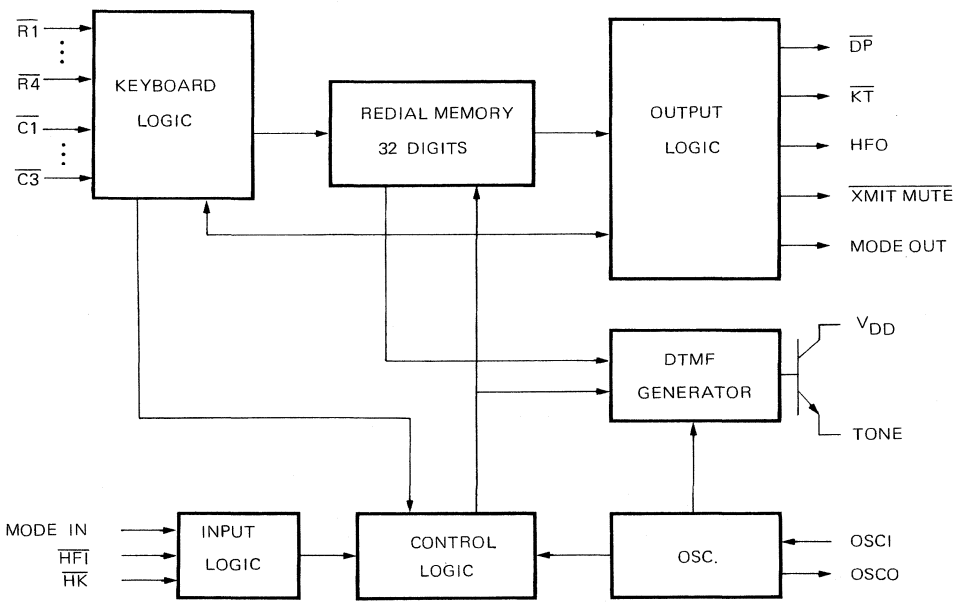


Keyboard Assignment



1. */T -- At Pulse mode this key works as Pulse → DTMF key (T key), at DTMF mode the key works as *key. */T key will occupy one memory digit in either use.
2. F1 -- Flash key. The break time is 297 ms or 96 ms (UM91214/15 respectively)
3. F2 -- Flash key for break time 640 ms
4. P -- Pause key (2.2 seconds)
5. RD -- One key redial key
6. # -- At pulse mode this key input is neglected, at DTMF mode this key works as # key.

Block Diagram



Pin Descriptions

Pin No.				I/O	Symbol	Description
UM91215A UM91214A	UM91215B UM91214B	UM91215C UM91214C	UM91215D UM91214D			
3 4	3 4	4 5	4 5	I	OSCI OSCO	Oscillator Input and Output pins The time base for the UM91214/15 is a crystal controlled on – chip oscillator, which is completed by connecting a 3.58 MHz crystal or ceramic resonator between the OSCI and OSCO pins.
2	2	3	3	I, Z	MODE IN	Tri-State mode select pin. There are two versions of the UM91214/15. a. The UM91215 series is for European and American systems.

MODE IN	Tone/ Pulse	Dial Rate	M/B Ratio
V_{DD}	Pulse	10 pps	2/3
V_{SS}	Tone	–	–
Floating	Pulse	10 pps	1/2

b. The UM91214 series is for the Japanese system

MODE IN	Tone/ Pulse	Dial Rate	M/B Ratio
V_{DD}	Pulse	10 pps	1/2
V_{SS}	Tone	–	–
Floating	Pulse	20 pps	1/2

The mode selection pin is checked for tone/pulse dialing at each digit key entry. In pulse mode, the dialing rate is checked, along with the make/break ratio, at the first key entry.

1	1	2	2	I	$\overline{HK}$	Hook switch input. This inverter input pin detects the state of the hook switch contact. "Off Hook" is represented by a V_{SS} condition. "On Hook" is represented by a V_{DD} condition.

Pin Descriptions (Continued)

<table>
<tr><th colspan="4">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">Symbol</th><th rowspan="2">Description</th></tr>
<tr><th>UM91215A
UM91214A</th><th>UM91215B
UM91214B</th><th>UM91215C
UM91214C</th><th>UM91215D
UM91214D</th></tr>
<tr><td>(N. A.)</td><td>10</td><td>(N. A.)</td><td>11</td><td>O</td><td>$\overline{KT}$</td><td>Key-in tone output
This N-channel open drain pin sends out a "beep" tone for each pulse mode key entry, along with entries of accepted function keys (RD, T, F1, F2, and P keys). The tone output frequency is 437 Hz and tone duration is 23 ms.</td></tr>
<tr><td>9</td><td>11</td><td>10</td><td>12</td><td>O</td><td>$\overline{DP}$</td><td>Dialing pulse output.
This is an N-channel open drain output. The normal output will be "ON" during break and "OFF" during make in the pulse dialing mode.</td></tr>
<tr><td rowspan="2">(N. A.)</td><td rowspan="2">(N. A.)</td><td>1</td><td>1</td><td>O</td><td>HFO</td><td rowspan="2">Hands Free Control I/O pins.
These pins enable and disable the Hands Free Control function. When input pin HFI goes low, the Hands Free Control state is toggled on. Status of the Hands Free Control state is listed in the following table:

<table><tr><th colspan="2">Current State</th><th colspan="3">Next State</th></tr><tr><td>Hook sw.</td><td>HFO</td><td>Input</td><td>HFO</td><td>Dialing?</td></tr><tr><td>—</td><td>Low</td><td>$\overline{HFI}$ ↓</td><td>High</td><td>Yes</td></tr><tr><td>On Hook</td><td>High</td><td>$\overline{HFI}$ ↓</td><td>Low</td><td>No</td></tr><tr><td>Off Hook</td><td>High</td><td>$\overline{HFI}$ ↓</td><td>Low</td><td>Yes</td></tr><tr><td>On Hook</td><td>—</td><td>Off Hook</td><td>Low</td><td>Yes</td></tr><tr><td>Off Hook</td><td>Low</td><td>On Hook</td><td>Low</td><td>No</td></tr><tr><td>Off Hook</td><td>High</td><td>On Hook</td><td>High</td><td>Yes</td></tr></table></td></tr>
<tr><td>18</td><td>20</td><td>I</td><td>$\overline{HFI}$</td></tr>
<tr><td>7</td><td>7</td><td>8</td><td>8</td><td>O</td><td>Tone</td><td>Tone dialing output.
When a valid keypress is detected in the DTMF mode, appropriate low group and high grop frequencies are generated which hybridize the dual tone output. TONE OUT is in the "OFF" state in pulse mode.</td></tr>
</table>

Pin Descriptions (Continued)

Pin No.				I/O	Symbol	Description
UM91215A UM91214A	UM91215B UM91214B	UM91215C UM91214C	UM91215D UM91214D			
8	8	9	9	O	$\overline{\text{XMITMUTE}}$	Dialing transmission mute output. This is an N-channel open drain output. Normally, the transmission mute output is "OFF" during pulse or DTMF dialing this output is "ON".
(N. A.)	9	(N. A.)	10	O	MODE OUT	Mode output pin. This is an N-channel, open drain output. It is "ON" during tone output and "OFF" during pulse output.
13	15	14	16		$\overline{R1}$	Keyboard pins. This input serves as the interface to an XY matrix keyboard. On a 4 x 4 matrix keyboard, the input from the fourth column, $\overline{c4}$, should be connected to V_{SS}.
14	16	15	17		$\overline{R2}$	
15	17	16	18		$\overline{R3}$	
16	18	17	19		$\overline{R4}$	
10	12	11	13		$\overline{C1}$	
11	13	12	14		$\overline{C2}$	
12	14	13	15		$\overline{C3}$	
6	6	7	7		V_{DD}	Power supply pins. This device is designed to operate from 2.0V to 5.5V
5	5	6	6		V_{SS}	

Description of Operation

In the description below, signals are defined in terms of the key or switch which is activated.

[Off Hook] means the phone was taken off the hook.
[On Hook] means that the receiver is on the hook.
[D1] stands for the first digit dialed in a string of digits.
[Dn] stands for the last digit dialed in a string of digits.
[Dn+1] stands for the beginning of a new string of digits.
[Dn+m] stands for the last digit in a new string of digits.
[$\overline{\text{HFI}}\downarrow$] stand for the switch that activates the Hands Free dialing mode going low.
[*/T] is the Pulse-to-DTMF key.
[RD] is the Redial key.
[0] is the Zero key.
[P] is the Pause key.
[F] is the Flash key.

1. Pulse mode operation

a. [Off Hook] [D1] . . . . . [Dn]

Pulse mode is defined as the initial mode, provided the first keyboard input is not the [*/T] key following the [Off Hook] condition and the mode selection pin is floating (MODE IN = V_{DD} or floating)

b. [On Hook] [$\overline{\text{HFI}}\downarrow$] [D1] . . . . [Dn]

Pulse mode is defined as the initial mode, provided the key input [D1] is not [*/T] while the mode selection pin is V_{DD} or floating. The chip will pause for 824 ms automatically after it detects an [Off Hook] condition or the [$\overline{\text{HFI}}\downarrow$] key is depressed. It then proceeds with pulse or DTMF dialing if any keys have been depressed.

The dialing rate or make/break ratio is decided at the first key entry by checking the MODE IN status and will not be altered. The MODE IN status can only switch the dialing mode from Pulse to DTMF after the first key entry.

2. DTMF mode operation

   a. Off Hook | D1 | ..... | Dn | or
   On Hook | HFI ↓ | D1 | ..... | Dn

   DTMF mode is defined as the initial mode of the mode selection pin MODE IN is V_{SS}.

   b. Off Hook | */T | D1 | ..... | Dn | or
   On Hook | HFI ↓ | */T | D1 | ..... | Dn

   The initial mode is pulse mode if the mode selection pin, MODE IN, is V_{DD} or floating. The */T key can switch the dialing mode to tone mode. Unlike normal mode switching, the */T key entry, as the first key pressed, will not produce any pause time. There are only 31 digits of redial memory available in the buffer to be used for operations a and b, since the mode switching key, */T, will occupy one digit of space.

3. Manual dialing with automatic access pause

   Off Hook | O | P | D1 | ..... | Dn

   Pause key entries can be accepted and stored in the redial memory. Each is stored as a digit. Each key-in will provide a pause of 3.57 seconds, depending on which model you are using.

4. Redial

   a. Off Hook | RD | or | On Hook | HFI ↓ | RD |

   Up to 32 digits (in pulse mode) or 31 digits (in tone mode) can be dialed using the RD key. The RD key is disabled while pulse or tone signals are being transmitted. Redial will also be inhibited if the last number dialed exceeds 32 digits because the redial memory can only hold 32 digits.

   b. Off Hook | RD | D1 | ..... | Dn | or
   On Hook | HFI ↓ | RD | D1 | ..... | Dn

   After pressing the RD key, we can add digits to the number in redial memory. When finished dialing, the redial memory will contain the original digits plus the digits dialed after pressing RD. Each time the redial key is pressed, the stored number will be dialed exactly the same as it was previously, regardless of the status of the MODE IN pin.

5. TONE/PULSE switching operation

   a. Off Hook | D1 | ..... | Dn | MODE IN pin
   ← Pulse Mode →
   switched to VSS | Dn+1 | .... | Dn+m
   → | ← DTMF Mode →

   The mode selection pin is always checked for tone or pulse mode key entry. Dialing can be switched from pulse to tone mode, but not from tone to pulse mode. Switching the MODE IN pin to V_{SS} will cause the chip to store a */T digit prior to the first tone digit in the redial memory and will automatically insert a 2.2 second pause before the tone digits are dialed out. After the mode has been switched, the status of the mode selection pin will no longer be checked. Therefore, it will not be possible to switch from tone to pulse mode.

   b. Off Hook | D1 | ..... | Dn | */T | Dn+1
   ← Pulse Mode →|←
   ..... | Dn+m
   DTMF Mode →|

   Pulse mode is initially defined with the mode selection pin, MODE IN, equal to V_{DD} or floating. At this time, the mode can be switched to DTMF by pressing the */T key. DTMF mode will begin as soon as the last pulse has been transmitted. In this mode, Dn+1 through Dn+m are sent through the TONE OUT pin as DTMF signals. If a P key entry is contained in the series of digits before or after the */T entry, or the MODE IN switch is depressed, 2.2 second pause will be added to the automatically inserted pause time, which is also 3.57 seconds. Both of the above switching modes can store as many as 31 digits in the redial memory.

6. One-Key redialing

   Off Hook | D1 | ..... | Dn | RD | or
   On Hook | HFI ↓ | D1 | ..... | Dn | RD

   If the dialing of D1 to Dn is finished, pressing RD will cause the pulse dialing pin to go low for 2.2 seconds of break time and an 824 ms pause will automatically be added. If the pulses of the number dialed with D1 to Dn have not finished, the pressing of the redial key will be ignored.

7. Flash dialing

   Off Hook | F | D1 | ..... | Dn | or
   On Hook | HFI ↓ | F | D1 | ..... | Dn

   The flash keys emulate quick On-Off Hook operations. Pressing the flash keys, F1 or F2, will cause a break of 96 ms or 640 ms (or, 297 ms or 640 ms, depending on the model) on the $\overline{DP}$ output pin. Then, it pauses for 824 ms and continues dialing the digits, D1 to Dn. These digits are then stored in the redial memory.

   Each time the flash key is pressed, the redial memory will be cleared to store a new entry. In addition, the MODE IN status will be checked again for the setting of the Tone/Pulse dialing mode.

   Similarly, to make sure that the IC is working properly, new flash key inputs will be ignored as long as the digits that were dialed have not finished.

Absolute Maximum Ratings *

Supply Voltage (V_{DD}) . . . . . $\leqslant$ 6.0V
Input Voltage (V_{IN}) . . . . . V_{SS} − 0.3V to V_{DD} + 0.3V
Output Voltage (V_{OUT}) . . . . . V_{SS} − 0.3V to V_{DD} + 0.3V
Output Voltage (V_{OUT}) (DP, XMIT MUTE) . . . . $\leqslant$ 1.2V
Tone Output Current (I_{TONE}) . . . . . $\leqslant$ 50 mA
Power Dissipation (P_D) . . . . . $\leqslant$ 500 mW
Operating Temperature (T_{OP}) . . . . . −20°C to +70°C
Storage Temperature (T_{STG}) . . . . . −40°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 3.579545 MHz, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		Test CKT.
Operating Voltage	V_{DD}	2.0		5.5	V	Pulse mode		A
		2.0		5.5		Tone mode		
Memory Retention Voltage	V_{MR}	1			V			—
Memory Retention Current	I_{MR}		0.05	0.4	μA	V_{DD} = 1.0V, $\overline{HK}$ = V_{DD} All outputs unloaded		—
Operation Current	I_{DDP}		0.32	1.0	mA	Pulse mode	All outputs unloaded	A
	I_{DDT}		0.6	2.0		Tone mode		
Standby Current	I_{SO}		0.03	0.05	μA	$\overline{HK}$ = V_{DD} = 1.5V	All outputs unloaded No key selected	A
			0.5	10		$\overline{HK}$ = V_{SS}		
Input Voltage	V_{IH}	0.8		1	V_{DD}			
	V_{IL}	0		0.2				
$\overline{R1}$ ~ $\overline{R4}$ Input Current	I_R		115		μA			C
Tone out Voltage	V_{OC}	584	730	876	mV_{P-P}	Column	V_{DD} = 3.5V R_L = 5K	D
	V_{OR}	456	570	684		Row		
$\overline{HFI}$ Pull Low Current	$\|I_{HFI}\|$		5		μA	V_{DD} = 3.5V. (Note 1) $\overline{HFI}$ pin connected to 0V		
HFO Source Current	$\|I_{OH1}\|$	0.4	2		mA	V_{DD} = 3.5V V_{OH} = V_{DD} − 0.4V		B
HFO, $\overline{KT}$, MODEOUT $\overline{XMUTE}$ Sink Current	I_{OL1}	0.9	5.3		mA	V_{DD} = 3.5V V_{OL} = 0.4V		B
$\overline{DP}$ Sink Current	I_{OL2}	1.1	5.3		mA	V_{DD} = 3.5V V_{OL} = 0.4V		B
Distrotion	DIS %			10	%	*Note 1		

Note 1:

$$DIS\% = \frac{100 \cdot (V_1^2 + V_2^2 + \ldots + V_n^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$$

a. V_1 . . . . . V_n are the intermodulation or the harmonic frequencies in the 500 Hz to 3400 Hz band.

b. V_{IL} and V_{IH} are the individual frequency components of the DTMF signal.

AC Electrical Characteristics

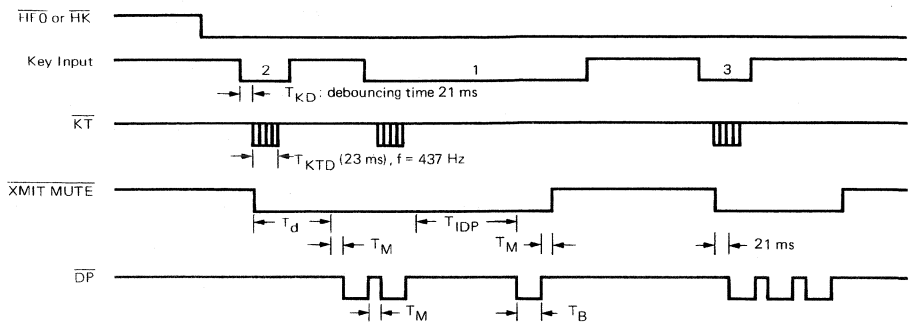
(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 3.579545 MHz T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Make Time	T_M	10 pps	M/B = 1/2		33.3		mS
			M/B = 2/3		40.0		
		20 pps	M/B = 1/2		16.7		
			M/B = 2/3		20.0		
Break Time	T_B	10 pps	M/B = 1/2		66.6		mS
			M/B = 2/3		60		
		20 pps	M/B = 1/2		33.3		
			M/B = 2/3		30		
Inter Digit Pause Time	T_{IDP}	10 pps			824		mS
		20 pps			458		
Pause Time	T_{PAU}				2.2		S
Auto-redial Break Time	T_{ROBK}	*Optional			2.2		S
Delay time Key valid to Signal out	T_d				0		mS
Key-in Debaunce	T_{KD}				21		mS
Key-in Tone Duration	T_{KTD}				23		mS
Key-in Tone Frequency	F_{KT}				437		Hz
Minimun Tone Duration Time	T_{MFD}				94		mS
Min. Tone Inter-digit Pause	T_{TIDP}				96		mS
Redial Tone Duration	T_{MFDR}				94		mS
Redial Tone Inter-digit Duration	T_{TIDPR}				96		mS

R/C	Conditions	spec.	Actual	Error (%)	Unit
$\overline{R1}$	F_{OSC} = 3.579545 MHz	697	699.1	+0.31	HZ
$\overline{R2}$		770	771.5	+0.19	HZ
$\overline{R3}$		852	852.3	+0.03	HZ
$\overline{R4}$		941	942.0	+0.10	HZ
$\overline{C1}$		1209	1,215.7	+0.57	HZ
$\overline{C2}$		1336	1,331.7	–0.32	HZ
$\overline{C3}$		1477	1,471.9	–0.35	HZ

Timing Waveform

1. Timing Waveform in pulse mode:



T_d : Delay time of Key valid to dialing signal out, typically 0 ms

T_{IDP} : Inter digit pause time

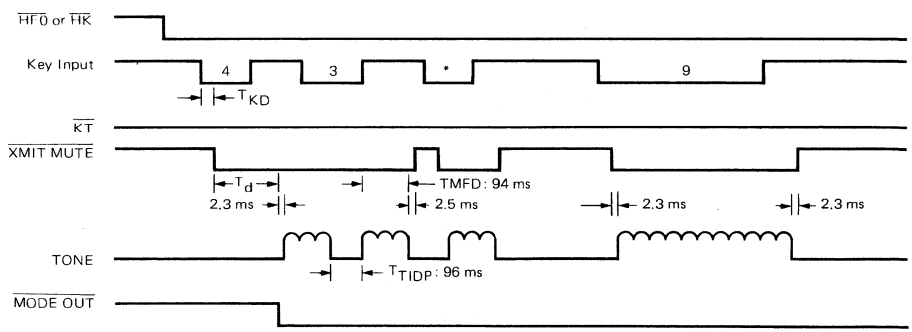
T_{KTD} : Key in tone duration

T_{KD} : Debouncing time

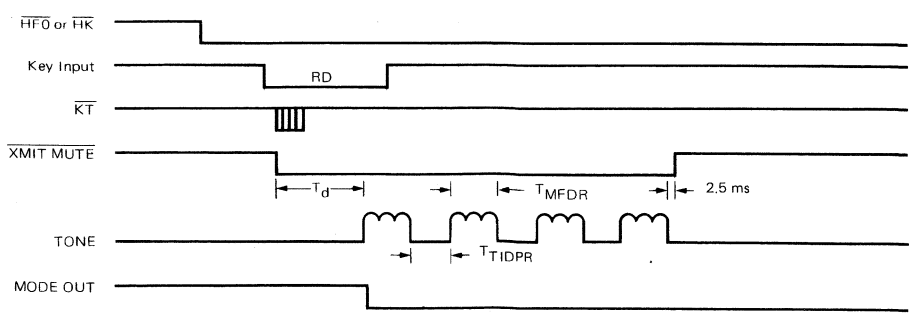
Note: "HK or HFO" indicates chip works when hook switch HK goes low or hands free control output HFO goes high.

2. Timing Waveform in tone mode:

(i) Normal dialing

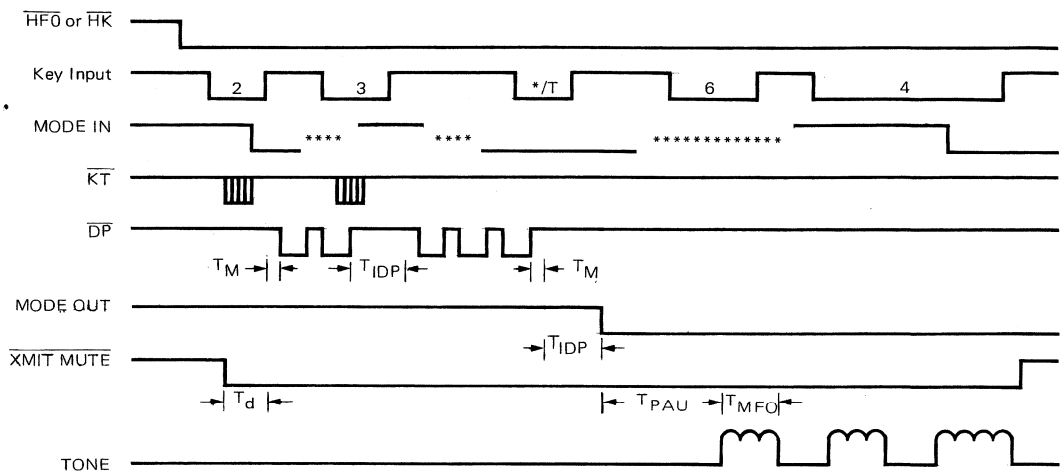


(ii) After (i), redialing

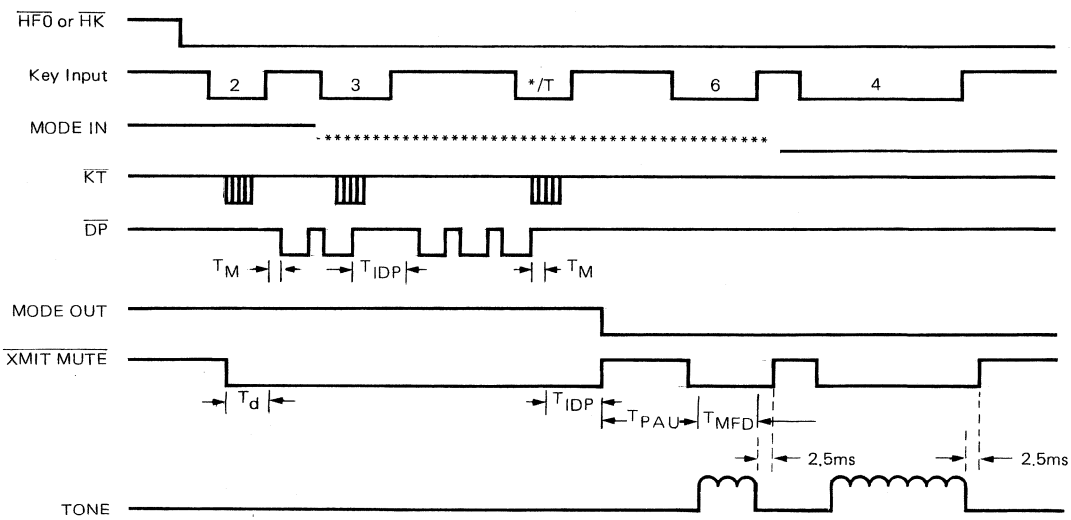


3. Timing Waveform for switching mode operation:

(i) By mode selection pin switches

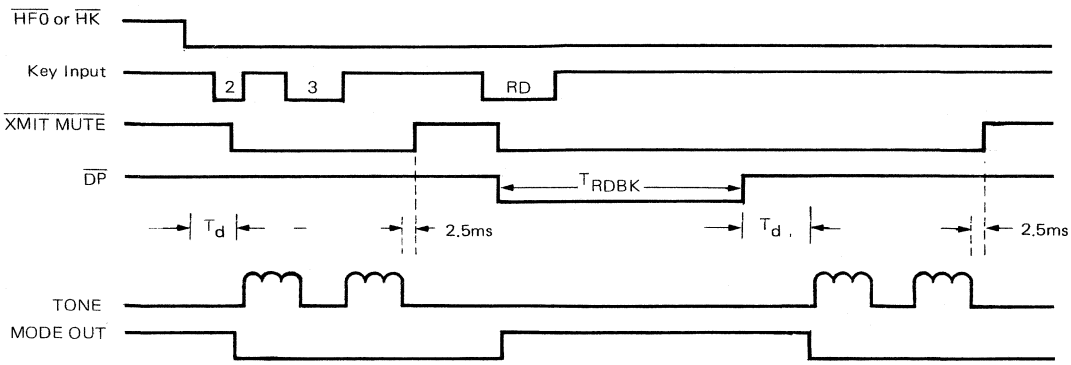


(ii) By */T key entry



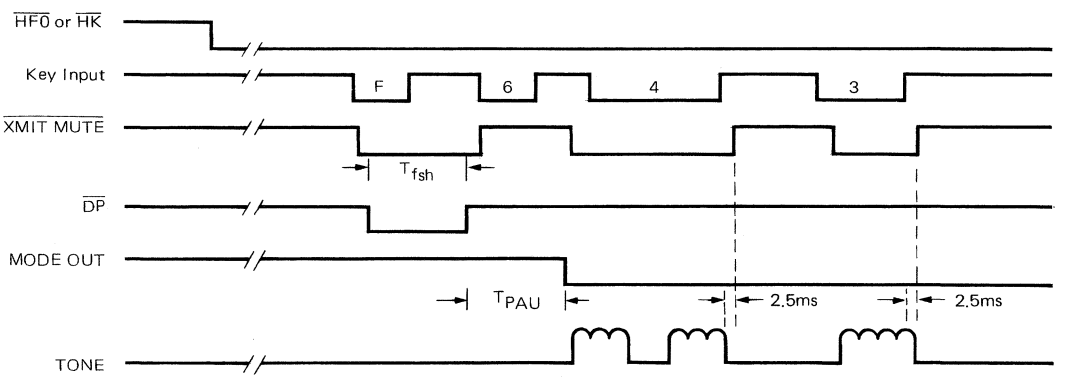
T_{PAD} : Pause time (2.2 secs)

4. One key redial (DTMF mode for example):



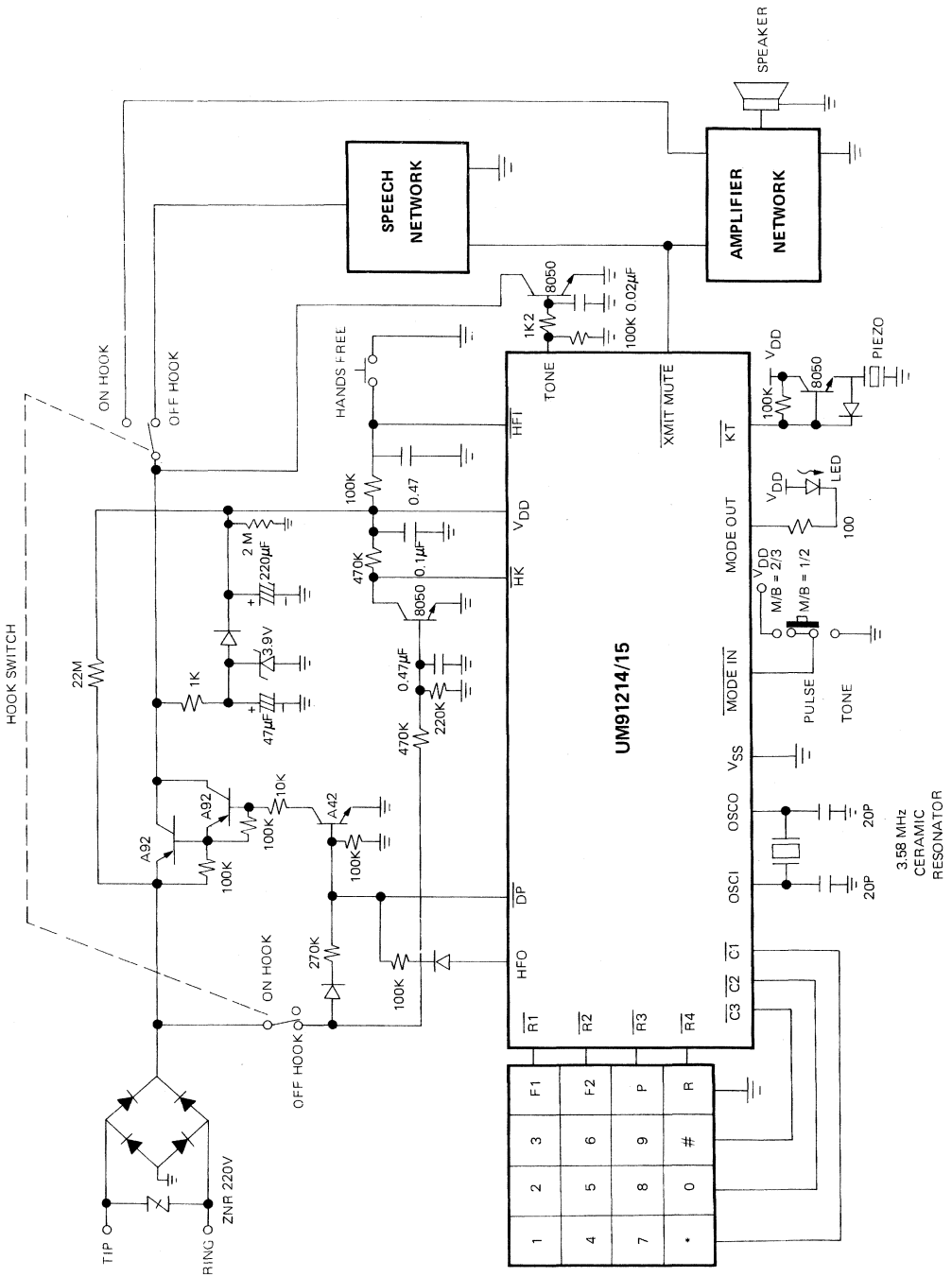
T_{RDBK} : Break time (2.2 secs)

5. Flash dialing (DTMF mode for example):



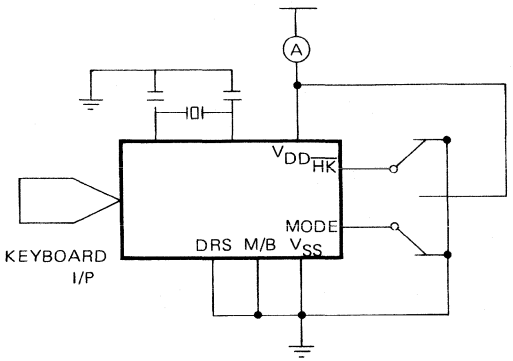
T_{fsh}: flash time 96 or 640 ms (F1 or F2 respectively) for UM91215
flash time 297 or 640 ms (F1 or F2 respectively) for UM91214

Application Circuit

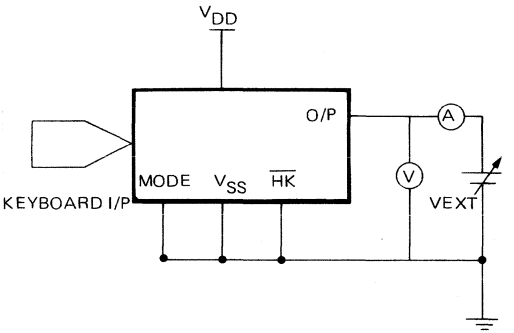


Test Circuits

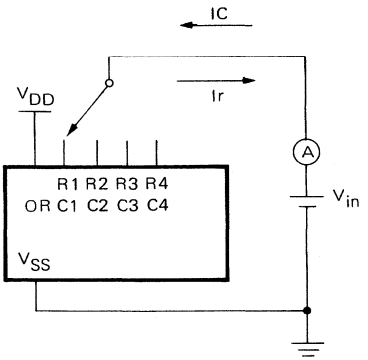
(A)



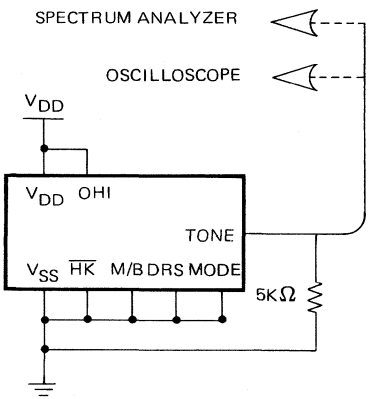
(B)



(C)



(D)



OSCILLOSCOPE: TEKTRONIX 468
SPECTRUM ANALYZER: HP 3585A

Ordering Information

Part No.	Package	Key Tone	Hands Free Control	Dial Rate	M/B ratio	Flash	
						F1	F2
UM91214A	16-pin DIP	N. A.	N. A.	10/20 pps	1/2	297 ms	640 ms
UM91214B	18-pin DIP	A	N. A.				
UM91214C	18-pin DIP	N. A.	A				
UM91214D	20-pin DIP	A	A				
UM91215A	16-pin DIP	N. A.	N. A.	10 pps	1/2, 2/3 Selectable	96 ms	640 ms
UM91215B	18-pin DIP	A	N. A.				
UM91215C	18-pin DIP	N. A.	A				
UM91215D	20-pin DIP	A	A				

N.A.: Not Available A: Available

UMC

UM91260/61

10 Memory Tone/Pulse Dialer

Features

- 32-digit redial memory (31 digits in tone mode)
- Ten indirect memories, 16 digits in pulse mode, 15 digits in tone mode
- Tone/Pulse mode switching via slide switch (4.1 second pause inserted automatically)
- Wide operating voltage: 1.8V ~ 5.5V
- Uses 480 KHz ceramic resonator
- Low memory retention current ($\leqslant$ 0.1 μA at V_{DD} = 10V, $\overline{HK}$ = 1)
- Selectable Make/Break ratio
- Selectable dialing rate (UM91261 only)
- Key-in tone output for valid keypad entry recognition (UM91261 only)

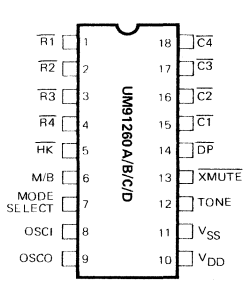
General Description

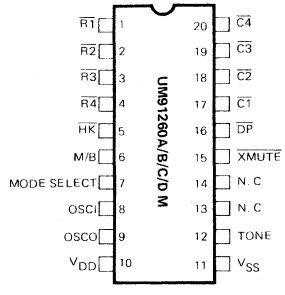
The products in the UM91260/61 series are tone/pulse switchable dialers with ten 16-digit number memories and 32-digit redial memory. Pulse to tone mode switching is performed via a slide switch. The dialing rate and storage mode for each version of the UM91260 is shown at right. The UM91261 is a 22-pin version of the 91260 with key-in tone output and selectable dialing rate and storage mode.

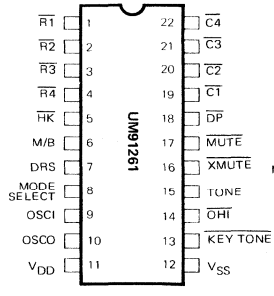
Ordering Information

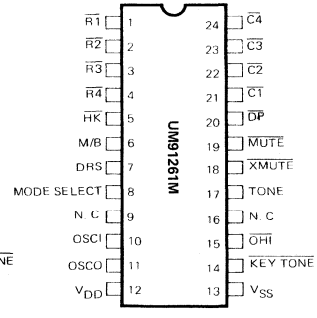
Part No.	Dialing rate	Storage mode	Package
UM91260A/60AM	10 pps	Off-hook only	P-DIP 18L/ SO 20L
UM91260B/60BM	20 pps	On/Off-hook	P-DIP 18L/ SO 20L
UM91260C/60CM	10 pps	On/Off-hook	P-DIP 18L/ SO 20L
UM91260D/60DM	20 pps	Off-hook only	P-DIP 18L/ SO 20L
UM91261/61M	Pin Selectable	Pin Selectable	P-DIP 22L/ SO 24L

Pin Configurations

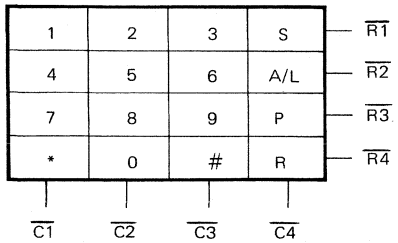






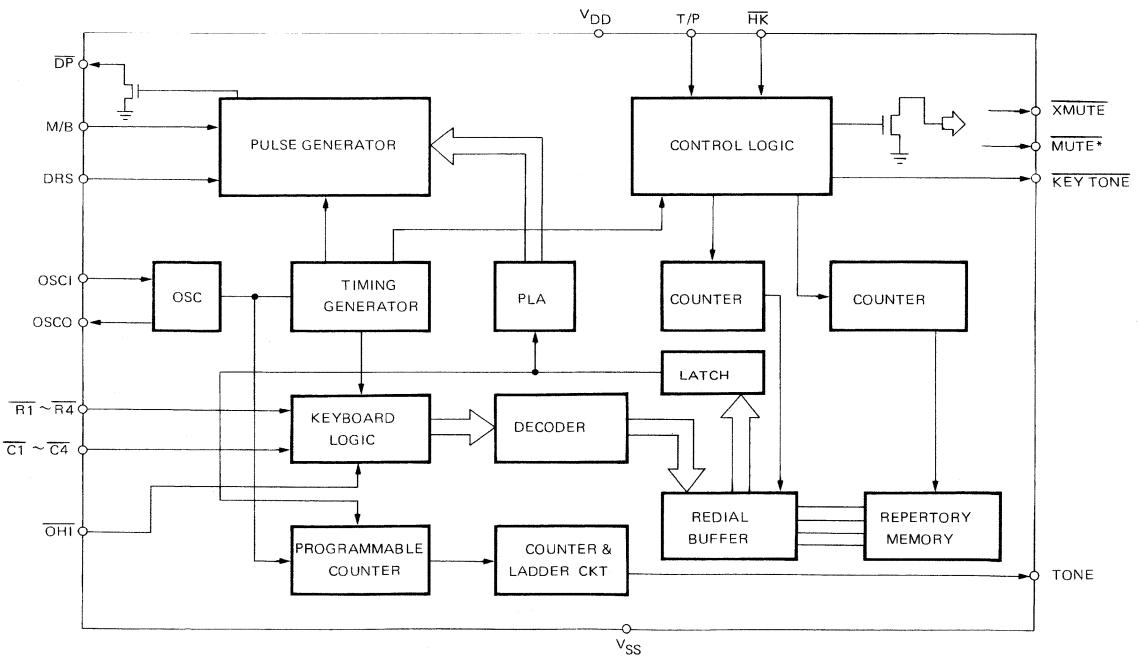


Keyboard Assignments



S: Store
A/L: Auto/Location
P: Pause
R: Redial

Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage . . . . . –0.3V to +6.0V
Input Voltage . . . . . –0.3V to V_{DD} + 0.3V
Maximum Power Dissipation (at 25°C) . . . . . 500 mW
Operating Temperature (T_{OP}) . . . . . –20°C to +70°C
Storage Temperature (T_{STG}) . . . . . –55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 480 KHz, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD}	1.8		5.5	V	Pulse mode	A
		1.8		5.5		DTMF Mode	
Memory Retention Voltage	V_{MR}	1			V		–
Memory Retention Current	I_{MR}		0.05	0.4	μA	V_{DD} = 1.0V All outputs unloaded $\overline{HK}$ = V_{DD}	–
Supply Operating Current	I_{DDP}		0.25	0.5	mA	Oscillator running; all outputs unloaded	A
	I_{DDT}		0.46	1.0			
Standby Current	I_{SD}		1.0	5.0	μA	$\overline{HK}$ = V_{SS} V_{DD} = 2.5V All outputs unloaded	A
Output Sink Current $\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$	I_{OL1}	1.0	2		mA	V_{OL} = 0.4V	B
	I_{OL2}	0.4	1		mA	V_{OL} = 0.4V V_{DD} = 2.0V	
Input Voltage Range	V_{IH}	0.8		1	V_{DD}		–
	V_{IL}	0		0.2			
Row Input Current	I_R	5	10	20	μA	V_{IN} = 0V All outputs unloaded	C
Column Input Current	I_C	0.6	1.4	2.0	mA	V_{IN} = 3.5V All outputs unloaded	C
Single Column Tone Output Amplitude	V_{OC}	540	590	640	mV_{P-P}	R_{LOAD} = 10 KΩ V_{DD} = 2.5V	D
		100	1200	1300		R_{LOAD} = 10 KΩ V_{DD} = 5.5V	D
Single Row Tone Output Amplitude	V_{OR}	410	450	490	mV_{P-P}	R_{LOAD} = 10 KΩ V_{DD} = 2.5V	D
		850	920	990		R_{LOAD} = 10 KΩ V_{DD} = 5.5V	D
Pre.-emphasis	T_{WIST}	1	2	3	dB		D
Valley of Single Tone	V_V	0.40	0.46	0.52	V_{DD}		D
Distortion	DIS%		1	5	%	*Note 1	D

Note 1: $$DIS(\%) = \frac{100 \cdot (V_1^2 + V_2^2 + \ldots + V_n^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$$

a. $V_1 \ldots V_n$ are the intermodulation or the harmonic frequencies in the 500 Hz to 3400 Hz band.

b. V_{IL}, V_{IH} are the individual frequency components of the DTMF signal.

AC Characteristics

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
PULSE							
Make/Break Ratio	M/B	M/B Terminal = V_{DD}			1/2		
		M/B Terminal = V_{SS}			2/3		
Dial Pulse Rate	DR	DRS = V_{DD} (20 pps Selection)			20		PPS
		DRS = V_{SS} (10 pps Selection)			10		
Make Time	T_M	10 pps	MB = 1/2		33.3		ms
			MB = 2/3		40.0		
		20 pps	M/B = 1/2		16.7		
			M/B = 2/3		20.0		
Break Time	T_B	10 pps	M/B = 1/2		66.6		ms
			M/B = 2/3		60		
		20 pps	M/B = 1/2		33.3		
			M/B = 2/3		30		
Inter-Digit Pause Time	T_{IDP}	10 pps	M/B = 1/2		806		ms
			M/B = 2/3		800		
		20 pps	M/B = 1/2		523		
			M/B = 2/3		520		
Pre-Digit Pause	T_{PDP}	10 pps	M/B = 1/2		840		ms
			M/B = 2/3		840		
		20 pps	M/B = 1/2		540		
			M/B = 2/3		540		
$\overline{\text{XMUTE}}$ $\overline{\text{MUTE}}$ DELAY Time	T_{MDP}	10 pps	M/B = 1/2		0		ms
			M/B = 2/3		0		
		20 pps	M/B = 1/2		0		ms
			M/B = 2/3		0		
TONE							
Minimum Tone Duration	T_{MFD}				110		ms
Min. Tone Inter-Digit Pause	T_{TIDP}				110		ms
Tone Output Pre-Digit Pause	T_{TPDP}				130		ms
$\overline{\text{XMUTE}}$ Delay Time	T_{MDT}				110		ms
Auto Pause Time	T_{AP}				4.1		S
Oscillator Start-up Time	T_{START}				8		ms

AC Characteristics (Continued)

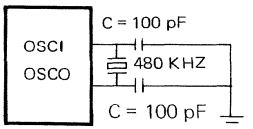
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{X\ MUTE}$, $\overline{MUTE}$ Start-up Time	T_{MS}			30		ms
KEY-IN						
Keypad Debounce Time	T_{KD}			22		ms
Key Scan Frequency	F_{KS}	$\overline{C1} \sim \overline{C4}$, $\overline{R1} \sim \overline{R4}$		377		Hz
KEY-IN TONE						
KT. Duration Time	T_{KTD}			42		ms
KT Frequency	F_{KT}			1.2		KHz
KT Start-up Time	$T_{KTSTART}$			30		ms

R/C	Conditions	Spec.	Actual	Error (%)	Unit
$\overline{R1}$	F_{OSC} = 480 KHz	697	695.65	–0.19	HZ
$\overline{R2}$		770	769.23	–0.1	HZ
$\overline{R3}$		852	851.06	–0.11	HZ
$\overline{R4}$		941	941.18	+0.02	HZ
$\overline{C1}$		1209	1212.12	+0.26	HZ
$\overline{C2}$		1336	1333.33	–0.2	HZ
$\overline{C3}$		1477	1481.48	+0.3	HZ

Pin Description

Pin No. 91260	Pin No. 91261	Designation	Description
1 2 3 4 15 16 17 18	1 2 3 4 19 20 21 22	$\overline{R1} \sim \overline{R4}$ $\overline{C1} \sim \overline{C4}$	Key inputs. When a row and a column are connected, a key operation is activated. If the On-Hook Store pin is inhibited, the row and column pins remain at high impedance in the On-Hook state. If the On-Hook Store pin is available, the column input is pulled low and the row input is pulled high. Scanning signals are present on both the row and column pins during a valid key-in condition. The key-in debounce time is typically 22 ms.
5	5	$\overline{HK}$	Hook switch input. When $\overline{HK} = V_{DD}$, an On-Hook state exists. When $\overline{HK} = V_{SS}$, an Off-Hook state exists.
6	6	M/B	Dial pulse Make/Break ratio select input. If M/B = V_{DD}, the Make/Break ratio is 1/2. If M/B = V_{SS}, the Make/Break ratio is 2/3.

Pin Description (Continued)

Pin No. 91260	Pin No. 91261	Designation	Description
–	7	DRS	Dialing rate select input. If DRS = V_{DD}, the dialing rate is 20 pps. If DRS = V_{SS}, the dialing rate is 10 pps.
7	8	MODE SELECT	Pulse/DTMF mode select input. If MODE SELECT = V_{DD}, Pulse mode is in effect. If MODE SELECT = V_{SS}, DTMF mode is in effect.
8 9	9 10	OSCI OSCO	Oscillator I/O. A 480 KHz ceramic resonator and two 100 pF serial loading capacitors form a complete oscillator circuit. The circuit is activated when $\overline{HK}$ is low. Oscillator start-up time is typically 10 ms. 
10 11	11 12	V_{DD} V_{SS}	Positive power supply. Negative power supply. Operating voltage range: Pulse mode = 1.8V to 5.5V DTMF mode = 1.8V to 5.5V
–	13	$\overline{\text{KEY-TONE}}$	Key-in tone output. This output is valid for both Pulse and Tone modes. Output frequency is 1.5 KHz and has a duration of 42.6 ms after a valid key-in is detected. This function is only available on the UM91261.
–	14	$\overline{\text{OHI}}$	On-Hook store. On-hook store function is available when this input is high, inhibited when this input is low.
12	15	TONE	DTMF signal output. Pull-down load resistance is 10,000Ω. The minimum tone and IDP durations are built-in for both normal dialing and redialing.
13	16	$\overline{\text{X MUTE}}$	Transmit mute output. This is an N-channel open drain output. The output transistor is switched on while a sequence of digits is being dialed (for both Pulse and Tone modes). Otherwise, it is switched off.
–	17	$\overline{\text{MUTE}}$	Mute output. This is an N-channel open drain output. The output transistor is switched on while a sequence of pulse digits is being dialed. Otherwise, it is switched off.
14	18	$\overline{\text{DP}}$	Dial pulse output. This pin is an N-channel open drain output. When $\overline{DP}$ output is low (switched on), it serves as a break signal in Pulse dialing. For other operations, $\overline{DP}$ output is normally high impedance (switched off).

Operational Procedures

9-1 Symbol definitions

a. D_P: Pulse digit, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0

b. D_t: tone digit, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #

c. LOCi: i = 1, 2, 3, 4, 5, 6, 7, 8, 9, 0

d. ZiZiZi: Conversation mode

e. 0–0↑ : OFF-HOOK

f. 0–0↓ : ON-HOOK

g ⌐↑ : Input Level from Low to high

h. ↓¬ : Input Level from High to Low.

9-2 Recommended dialing, redialing, mixed dialing and storing operations

1. Normal dialing in pulse mode

   0–0 ↑ , D_P . . . D_P, ZiZiZi 0–0↓

2. Normal dialing in tone mode

   0–0 ↑ , D_t . . . D_t, ZiZiZi 0–0↓

3. Mixed dialing in pulse-to-tone mode

   0–0 ↑ , D_P . . . D_P MODE SELECT.

   ↓¬ D_t . . . D_t, ZiZiZi 0–0↓

4. Redialing

   0–0↑, D_P . . . . . D_P 0–0↓,0–0↑,
   R, ZiZiZi, 0–0↓

   0–0↑, D_t . . . . . D_t 0–0↓,0–0↑,
   R, ZiZiZi0–0↓

5. Storing Numbers to Repertory Memory

   (i) Off-hook Store 0–0↑, [S], D_P . . . D_P or D_t . . . D_t

   [A/L] , LOCi, 0–0↓

   (ii) On/Off-hook store: 0–0↓, [S], D_P. . .D_P or D_t. . .D_t

   [A/L] , LOCi,

6. Dialing from Repertory Memory

   0–0↑ , [A/L], LOCi, ZiZiZi 0–0↓

Functional Description

1. N-Channel Open Drain Output – $\overline{DP}$, $\overline{XMUTE}$, $\overline{MUTE}$,

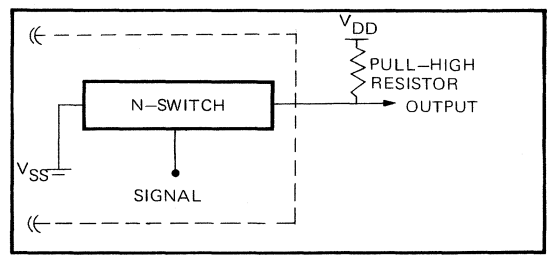


Figure. 1

2. DTMF Generator

   The digitally synthesized sinewave of the UM91260 series is well designed, with a 6 level, 12 segment, 1/2 V_{DD} reference voltage (see Fig. 2). The THD (Total Harmonic Distortion) of the DTMF output is typically 1%, when V_{DD} = 2.5V to 5.5V and frequency is in the 500 HZ to 3400 HZ band.

   DTMF Signal THD vs. operating voltage and DTMF output amplitude vs. operating voltage is shown in figures 3 and 4.

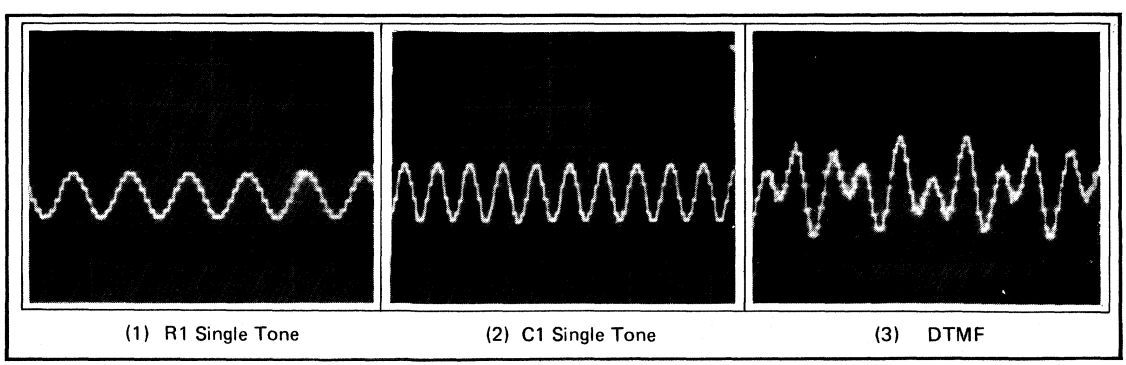
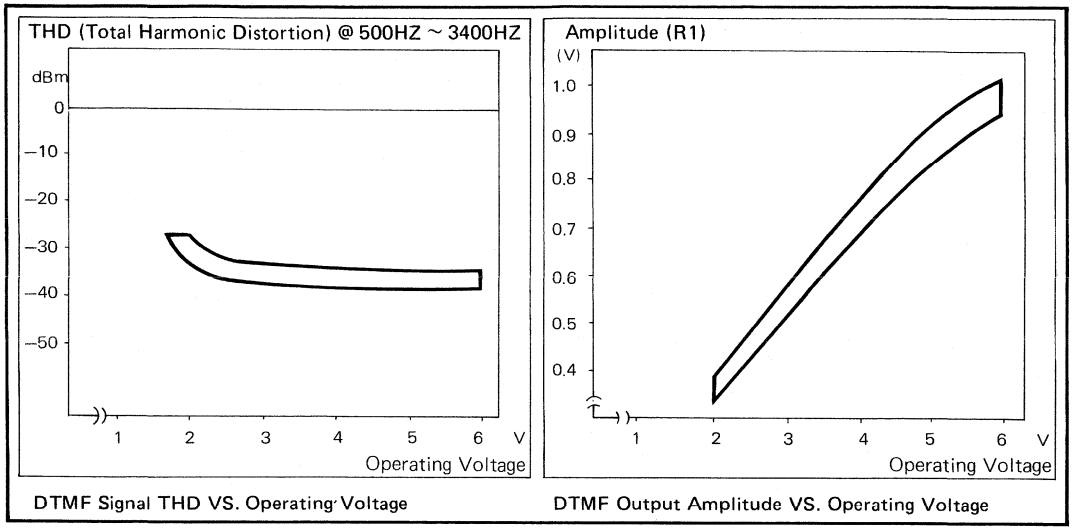


Figure 2 Waveforms



DTMF Signal THD VS. Operating Voltage

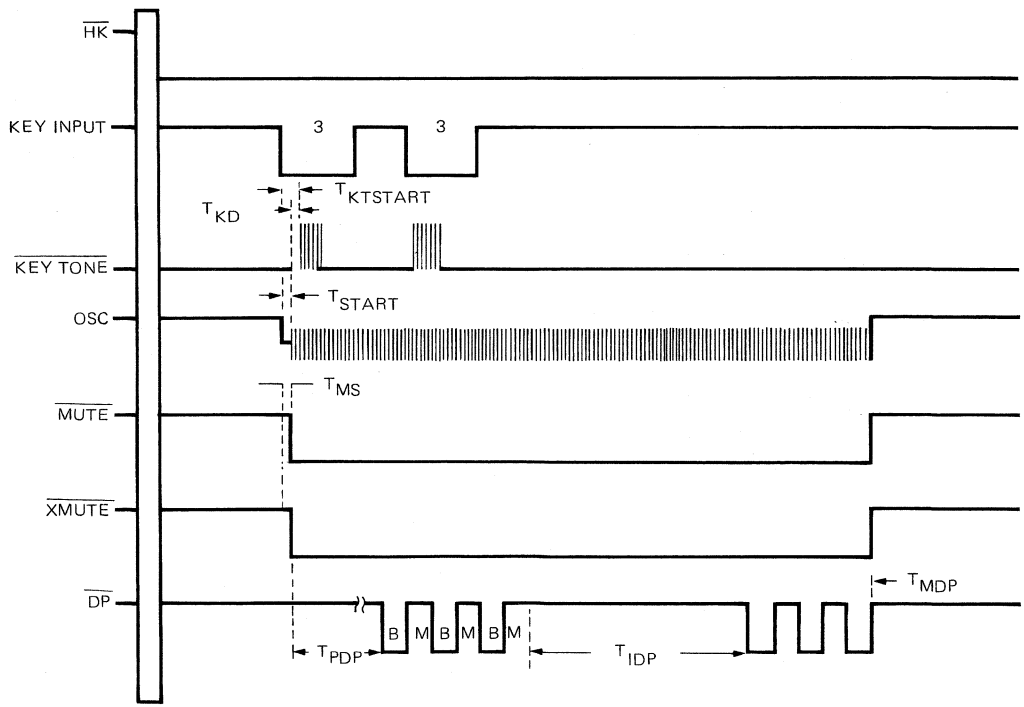
Figure 3

DTMF Output Amplitude VS. Operating Voltage

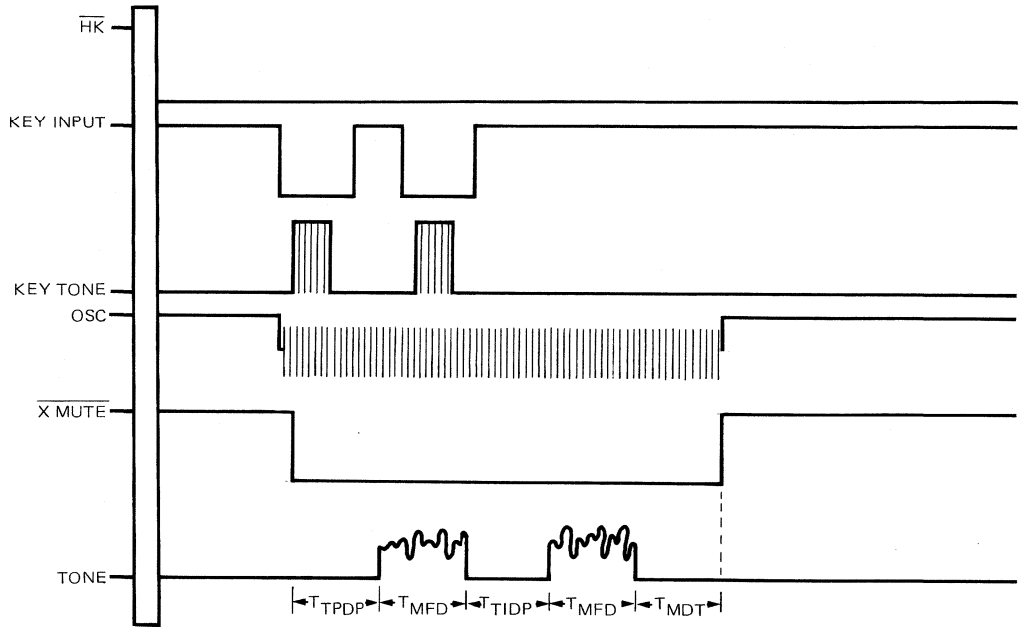
Figure 4

Timing Diagrams

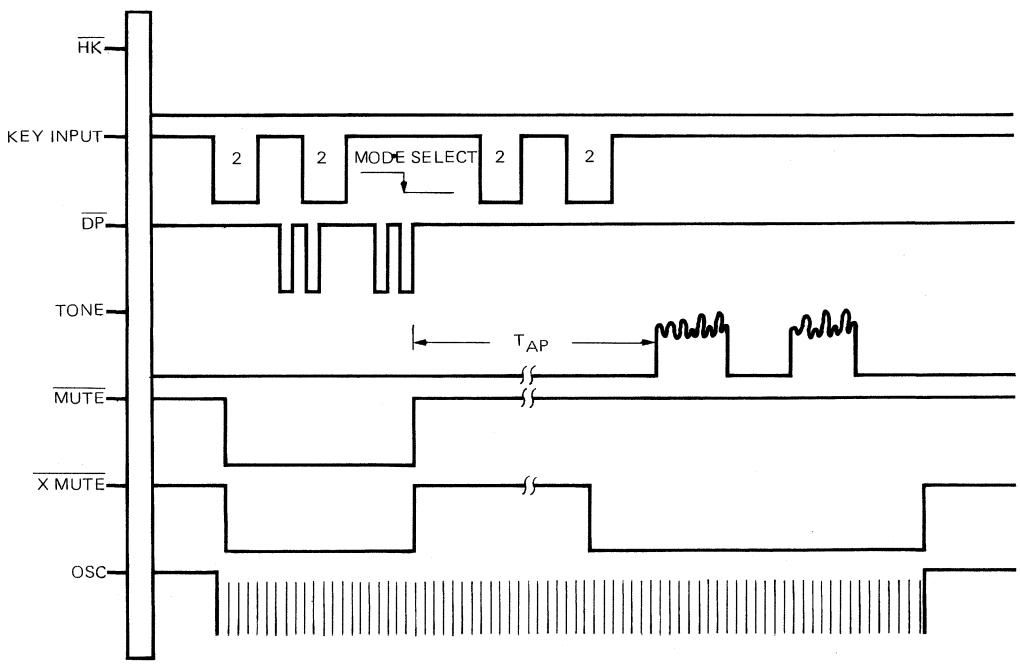
(1) PULSE MODE TIMING DIAGRAM



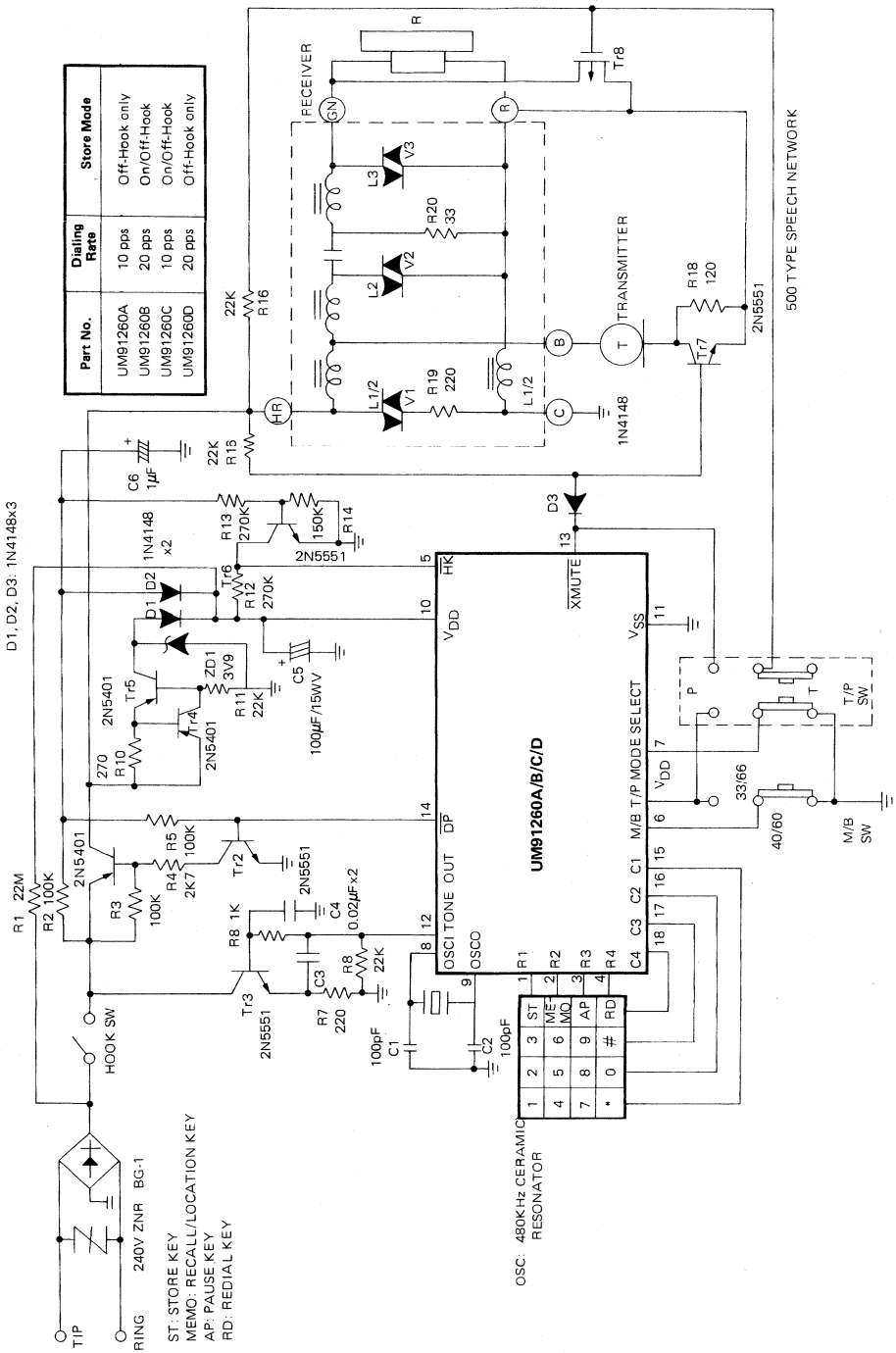
(2) TONE MODE TIMING DIAGRAM



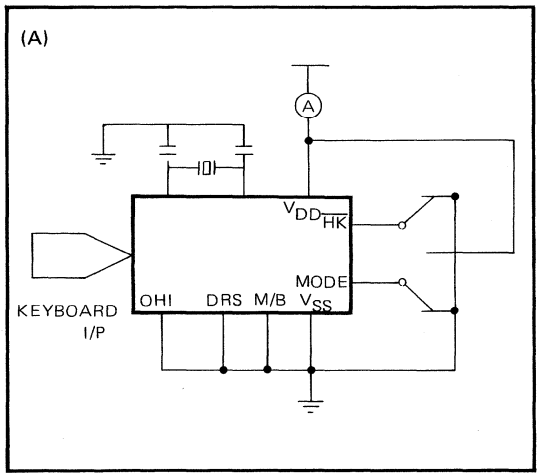
(3) NORMAL PULSE TO TONE MIXED DIALING VIA SLIDE SWITCH

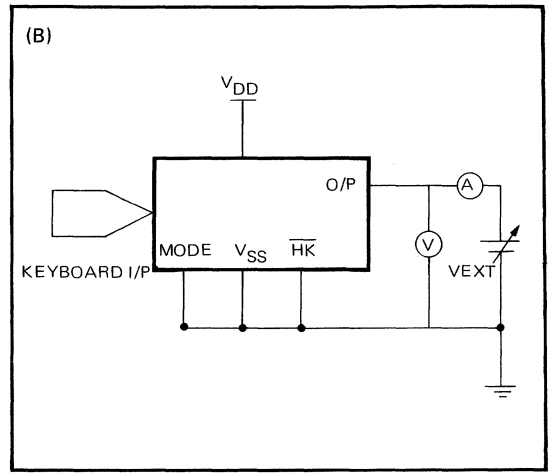


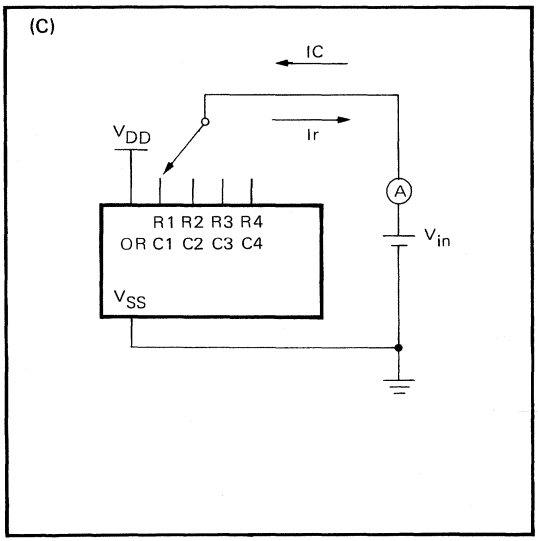
Typical Application Circuit

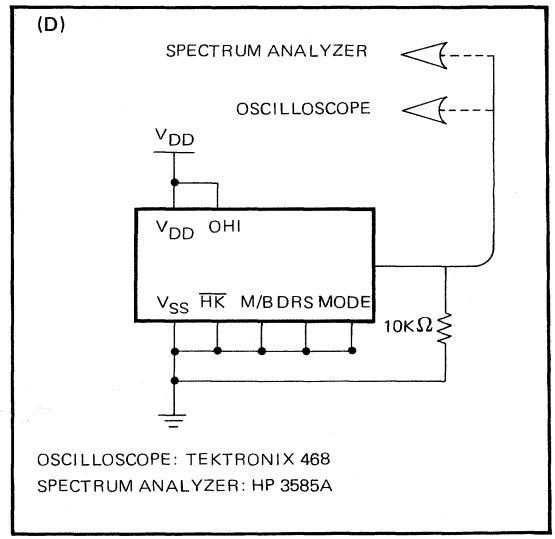


Test Circuits









UMC

UM91265

15 Memory Tone/Pulse Dialer

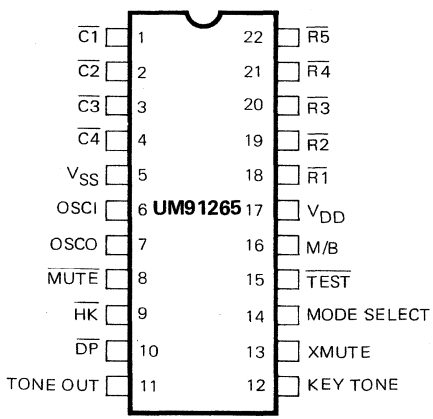
Features

- Tone/Pulse Switchable Dialer
- Stores ten 16-digit numbers for repertory dialing
- Additional four 16-digit numbers for emergency calls and long distance service company access code.
- One 31-digit Redial Memory
- Dialing length is unlimited, but if the normal dialing length of 31 digits is overstepped, then redial is inhibited
- Auto Pause Access for PBX and toll service operations; 3.1 seconds per pause
- Easy operation with Redial, Store, Auto and Pause keypads
- Key-tone output for valid keypad entry recognition
- Uses Form A keyboard or the standard 2-of-9 Matrix keyboard
- Electronic keypad input is available; low action
- Uses inexpensive 3.579545 MHz Television Color-burst crystal
- Pin selectable for make/break ratio
- Power-on reset is internally generated
- Memory Retention Current is less than 0.2μA at V_{DD} = 1.0V, on hook
- Wide operating voltage range: 2.0V to 5.5V
- Automatic switching from Pulse mode to Tone mode in long distance memory

General Description

The UM91265 is a monolithic integrated circuit which performs 15-memory tone/pulse switchable dialing functions for modern telephone set design. It is fabricated in CMOS technology and thus provides good performance in low voltage, low power operations. Four 16-digit direct dialing memories have been added for convenient emergency calls (such as fire, police, doctor, etc.) and long distance service company access code operations (such as MCI and SPRINT). A wide operating voltage range and low memory retention current facilitate this chip's excellent battery-free, direct line-powered operation.

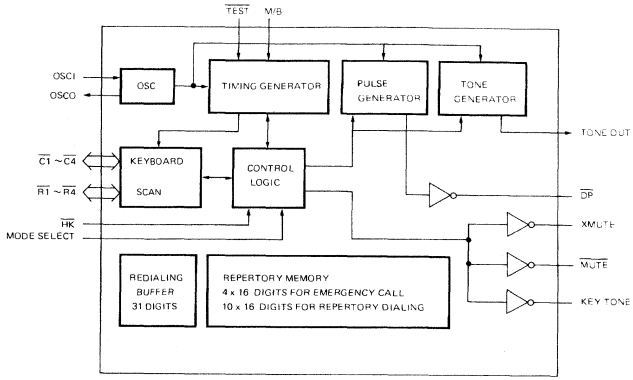
Pin Configuration & Keyboard Assignments



C1	C2	C3	C4	
1	2	3	EM1	R1
4	5	6	EM2	R2
7	8	9	EM3	R3
*	0	#	LDC	R4
R	S	A/L	P	R5

LDC : Long Distance Company
R : Redial
S : Store
A/L : Auto-Dial/Location
P : Pause

Block Diagram



Absolute Maximum Ratings*

DC Supply Voltage, V_{DD} 6.0V

Input Voltage Range, V_I . . . . . $-0.3V$ to $V^+ - 0.3V$

Power Dissipation Per Package, P_O (for $T_P = -25°C$ to $60°C$) 500mW

Operating Temperature, T_P . . . . . $-25°C$ to $85°C$

Storage Temperature, T_{stg} . . . . . $-65°C$ to $+150°C$

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

($V_{DD} = 3.5V$, $V_{SS} = 0V$, $F_{OSC} = 3.8$ MHz $T_{OP} = 25°C$ unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions	Test Ckt
		Min.	Typ.	Max.			
Operating Voltage	V_{DD}	2.0	–	5.5	V	Tone	
		2.0	–	5.5	V	Pulse	
		1.0	–	5.5	V	Memory	
Operating Current	I_{DD}	–	0.6	2	mA	Tone Notes 1, 4, 6	1
		–	0.2	0.5	mA	Pulse	
Memory Retention Current	I_R	–	0.1	0.2	μA	$\overline{HK} = 1$, $T_A = 45°C$, $V^+ = 1.0V$	2
Standby Current	I_S	–	0.1	5	μA	Notes 1, 2, 3, 5, 6	1
Tone Output Voltage	V_{TO}	130	150	170	mVrms	Row Group, $R_L = 10$ KΩ	3
Pre-emphasis		1	2	3	db	Column Group/Row Group $V_{DD} = 2.0$ to $5.5V$	4
DTMF Distortion	T_{HD}	–	–30	–23	db	$R_L = 10$ KΩ, Notes 7, 8	4
Tone Output External Load Impedance	R_L	10	–	–	KΩ	THD ≤ –23db	
Tone Output DC Level	V_{DD}	0.5		0.6	V^+	$V_{DD} = 2.5 - 5.5V$	4
Tone Output Sink Current	I_{TL}	0.2	–	–	mA	$V_{TO} = 0.5V$	5
Pulse Output Source Current	$\|I_{PH}\|$	0.2	–	–	mA	$V_{PO} = 2.0V$	5
Sink Current	I_{PL}	0.2	–	–		$V_{PO} = 0.5V$	6

DC Characteristics (Continued)

Parameter	Symbol	Limit			Unit	Conditions	Test Ckt
		Min.	Typ.	Max.			
Mute Output Source Current	$\|I_{MH}\|$	0.2	–	–	mA	V_{MO} = 2.0V	5
Sink Current	I_{ML}	2	–	–		V_{MO} = 0.5V	
Key Tone Output Source Current	$\|I_{KH}\|$	0.5	–	–	mA	V_{KO} = 2.0V	8
Sink Current	I_{KL}	0.5	–	–		V_{KO} = 0.5V	5
XMT Mute Source Current	$\|I_{LH}\|$	0.2	–	–	mA	V_{LO} = 2.0V	5
Sink Current	I_{IL}	0.2	–	–		V_{LO} = 0.5V	
Input Voltage Low	V_{IL}	GND	–	0.3	V^+	Pins 1-4, 9, 14, 15	
Input Voltage High	V_{IH}	0.7	–	–		16 & 18-22	
Keypad Input Source Current	$\|I_{KD}\|$	4	10	30	μA	V_I = 0V	6
Sink Current	I_{KS}	200	400	–	–	V_I = 2.5V	5, 7
Control Pin Input Leakage Current	I_{IN}	–	$\pm 10^{-5}$	± 0.1	μA	Pins 9, 14, 15, 16	

Note 1: $\overline{HK}$ = 0
Note 2: In DTMF Mode
Note 3: In Pulse Mode
Note 4: Keyboard Entry, Including Auto Dialing
Note 5: No Keyboard Entry
Note 6: All Outputs Unloaded
Note 7: Dual Tone Multi-Frequency Distortion is measured in terms of total out-of-band power related to sum of row and column fundamental power.
Note 8: Crystal parameters defined as Rs ⩽ 100Ω, Lm = 96mH, Cm = 0.25 pF, Ch = 5 pF, F = 3.579545 MHz and CL = 18 pF ΔF ⩽ ± 200 PPM

AC Characteristics

Crystal Parameter defined as RS ⩽ 100Ω, Lm = 96mH, Cm = 0.25 pF, Ch = 5 pF, F = 3.579545 MHz and C_L = 18 pF
ΔF ⩽ ± 200 PPM.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Pulse							
Make/Break Ratio	M/B	M/B = Terminal = V_{DD}			2/3		
		M/B Terminal = V_{SS}			1/2		
Dial Pulse Rate	DR	$\overline{TEST}$ Terminal = V_{DD}			10		pps
		$\overline{TEST}$ Terminal = V_{SS}			600		
Make Time	T_M	10 pps	MB = 2/3		40		mS
			MB = 1/2		33.3		
		600 pps	MB = 2/3		0.667		
			MB = 1/2		0.556		

AC Characteristics (Continued)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Break Time	T_B	10 pps	MB = 2/3		60		mS
			MB = 1/2		66.6		
		600 pps	MB = 2/3		1		
			MB = 1/2		1.111		
Inter-Digit Pause Time	T_{IDP}	10 pps	MB = 2/3		800		mS
			MB = 1/2		800		
		600 pps	MB = 2/3		13.3		
			MB = 1/2		13.3		
Pre-Digit Pause	T_{PDP}	10 pps	MB = 2/3		40		mS
			MB = 1/2		33.3		
		600 pps	MB = 2/3				
			MB = 1/2				
MUTE Delay	T_{MDP}	10 pps	MB = 2/3		40		mS
			MB = 1/2		33.3		
		600 pps	MB = 2/3				
			MB = 1/2				
TONE							
Minimum Tone Duration	T_{MFD}				100		mS
Minimum Tone Inter-Digit Pause	T_{TIDP}				105		mS
Key-In							
Key-In Debounce Time	T_{KD}	$\overline{TEST} = V_{DD}$			20		mS
Key-Release Debounce Time	T_{KR}				20		mS
Key Tone							
Key-Tone Frequency	F_{KS}	$\overline{C1} \sim \overline{C4}, \overline{R1} \sim \overline{R5}$			1.2		KHz

Row, Column Frequency

R/C	Spec.	Actual	Error (%)	Unit
R1	697	699	+0.29	Hz
R2	770	766	–0.78	Hz
R3	852	848	–0.47	Hz
R4	941	948	+0.74	Hz
C1	1209	1216	+0.58	Hz
C2	1336	1332	–0.30	Hz
C3	1477	1472	–0.34	Hz

Pin Description

Pin No.	Symbol	I/O	Description
1–4 18–22	$\overline{C1} \sim \overline{C4}$ $\overline{R1} \sim \overline{R5}$	I/O	The keypad input is compatible with the standard 2-of-9 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic inputs. Figure 1 shows how to connect the two keyboard types and Figure 2 shows wave forms for electronic inputs. In normal operation, any single button is pushed to produce a dual tone, pulses or a function. Activation of two or more buttons will result in no response, except for a single tone. Table 1 illustrates the address keypad function, in detail.
6 7	OSCI OSCO		A built-in inverter provides oscillation with an inexpensive 3.579545 MHz television color-burst crystal. The oscillator ceases when a keypad input is not sensed. An on-board counter is used to decrease the frequency of the oscillator and creates crystal debounce, mute delay, predigit pause, pulse rate, interdigit pause, Make/Break ratio, intertone pause, tone duration, row group and column group frequency, and key tone frequency oscillation. Any crystal frequency deviation from 3.579545 MHz will be reflected in the time parameter above. Most crystals do not vary more than ± 0.02 percent.
8	$\overline{MUTE}$	O	The $\overline{mute}$ is a conventional CMOS inverter that pulls to positive voltage with no keyboard input and pulls to ground when an address keypad entry is sensed (excluding the * and # keypads in pulse mode), that is, when any keypad in row 5 and column 4 is pushed, then mute out remains at high level. The mute output is used to cut out the current biased in type-2500 telephone circuit that is required to actuate upon address keypad input.
9	$\overline{HK}$	I	The $\overline{HK}$ (Hook Switch) input is used to sense the state of the handset as On-hook or Off-hook. In the On-hook state, $\overline{HK}$ = 1, the keyboard input is disabled. There is no operation for any keyboard entry. This avoids energy loss to the capacitor. In the Off-hook state, $\overline{HK}$ = 0, all of the functions work.
10	$\overline{DP}$	O	In the DTMF mode, the pulse out remains high regardless of keyboard entry. In the pulse mode, this output sends a chain of pulses to the corresponding keypad input address, but remains high for * and # entries. Figure 3 shows the timing diagram in pulse mode. Under normal conditions, the pulse rate and interdigit pause are fixed, Pin 15 = 1, and will be 10 pps and 800 ms respectively. The Make/Break ratio is pin selectable and depends on the state of the M/B pin. It is 60:40 for M/B = 1 and 66.6:33.3 for M/B = 0.
11	TONE OUT	O	This pin is used to send out the DTMF address code. During pulse dialing, it always remains in a low state, regardless of keypad input. In the tone mode, it will put out a single or dual tone. For a detailed description, please refer to Table 1. In normal dialing,, the tone duration depends on the length of key-in. When a keypad is held down less than 100 ms, the tone duration will remain fixed at 100 ms. If it is held down longer, the tone duration will last as long as key-in continues. The intertone pause will be different under the following conditions: when key release lasts less than 105 ms, the pause will be fixed at 105 ms; otherwise, it will be equal to the length of time the key was released. When redialing, the tone duration and intertone pause are internally set at 100 ms and 105 ms, respectively. Detailed timing diagrams of the tone modes are shown in Figures 4-(a) and (b).

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
12	KEY TONE	O	The key tone is from a conventional CMOS inverter. An NPN transistor is needed to drive the piezo. The output frequency is 1.2 KHz. No matter whether it is in DTMF or Pulse mode, the key tone will be accurate for any keypad entry (including row 5 and column 4) that is detected and will cease when the button is released. There will be no key tone output when two or more buttons on the keyboard are pushed simultaneously.
13	XMUTE	O	The XMUTE is a conventional CMOS inverter. An NPN transistor is used to turn off the LED. In the DTMF mode, output is actuated for the duration of DTMF signal transmission. But output remains low in pulse mode. In addition to controlling LED indication, it can also be used for muting operation in the Tone mode.
14	MODE SELECT	I	Pulls Pin 14 to V_{DD} when the dialer is in Pulse mode. Otherwise, it is in DTMF mode.
15	$\overline{TEST}$	I	In normal operation, the $\overline{TEST}$ pin is tied to V_{DD}, the single tone is inhibited and the pulse rate is 10 pps. During testing, the $\overline{TEST}$ pin is tied to ground, a single tone can be created by the method shown in Table 1, and all of the time parameters for pulse dialing are 60 times faster.
16	M/B	I	The Make/Break ratio is 2/3, if M/B = 1 and is 1/2 if M/B = 0. This pin influences nothing in the DTMF mode.
17 5	V_{DD} V_{SS}		Power supply pins. Operating voltage range: 2.0V ~ 5.5V

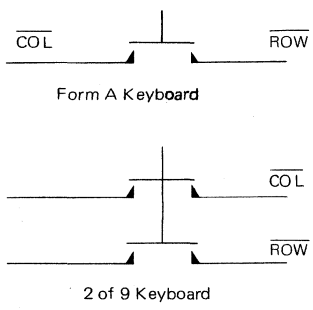


Figure 1. KEYBOARD CONFIGURATIONS

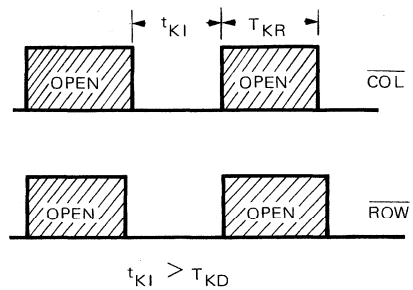


Figure 2. ELECTRONIC INPUTS

Table 1. Address Keypad Truth Table

Output		Active Low Inputs		Output
		$\overline{\text{ROW}}$ (Pins 18-21)	$\overline{\text{COLUMN}}$ (Pins 1-3)	Tone (Pin 11) Pulse (Pin 10)
Tone (Pin 14 = 0)	Normal (Pin 15 = 1)	One	One	Dual Tone
		Two or more	One	Pin 11 = 0
		One	Two or more	
		Two or more	Two or more	
	Single Tone (Pin 15 = 0)	One	One	Dual Tone
		Two or more	One	Column Tone
		One	Two or more	Row Tone
		Two or more	Two or more	Pin 11 = 0
Pulse (Pin 14 = 1)	10 pps (Pin15 = 1)	One	One	10 pps
		Two or more	One	Pin 10 = 1
		One	Two or more	
		Two or more	Two or more	
Pulse (Pin 14 = 1)	600 pps (Pin 15 = 0)	One	One	600 pps
		Two or more	One	Pin 10 = 1
		One	Two or more	
		Two or more	Two or more	

Note 1: In pulse mode, Pin 10 = 1 for * and # buttons.
Note 2: In pulse mode, Pin 11 always equals 0. In DTMF mode, Pin 10 always equals 1.
Note 3: Pin 10 = 1, Pin 11 = 0 for any button in Row 5 and Column 4, regardless of mode.

Operational Procedures

Symbol definitions

a. Dp: Pulse digit: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
b. Dt: Tone digit, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, *, #.
c. LOCi: Location i, i = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
d. ZiZiZi: conversation
e. 0-0 ↓: ON-HOOK
f. 0-0 ↑: OFF-HOOK
g. P: Pause Key
h. A/L: Auto-Dial/Location Key
i. R: Redially Key.
j. Emi: Emergency key i = 1, 2, 3.
k. S: Store key
l. LDC: Long Distance Call Key.

A. Normal dialing

1. Pulse mode

   0-0 ↑, DpDp . . . ZiZiZi 0-0 ↓
2. Tone mode

   0-0 ↑, DtDt . . . ZiZiZi 0-0 ↓

B. Redialing

0-0 ↑ DpDp . . . 0-0 ↓ 0-0 ↑
R, ZiZiZi: 0-0 ↓
0-0 ↑ DtDt . . . 0-0 ↓ 0-0 ↑
R, ZiZiZi: 0-0 ↓

C. Storing

S, DxDxDx . . . S, LOC i,

D. Memory dialing

0-0 ↑ A/L, LOCi, ZiZiZi, 0-0 ↓

E. Pause Key Operation

1. Storing with pause

   S, DxDxDx . . . P, DxDxDx . . . , S, LOCi

2. Dialing with Pause
   0−0 ↑ A/L, LOCi, ZiZiZi, 0−0 ↓
   Note: Every pause occupies one digit. Pause digit can be stored many times.

F. Emergency dialing

1. Storing emergency numbers.
   S, DxDxDx . . . ., S, Emi
2. Emergency dialing
   0−0 ↑, Emi, ZiZiZi, 0−0 ↓

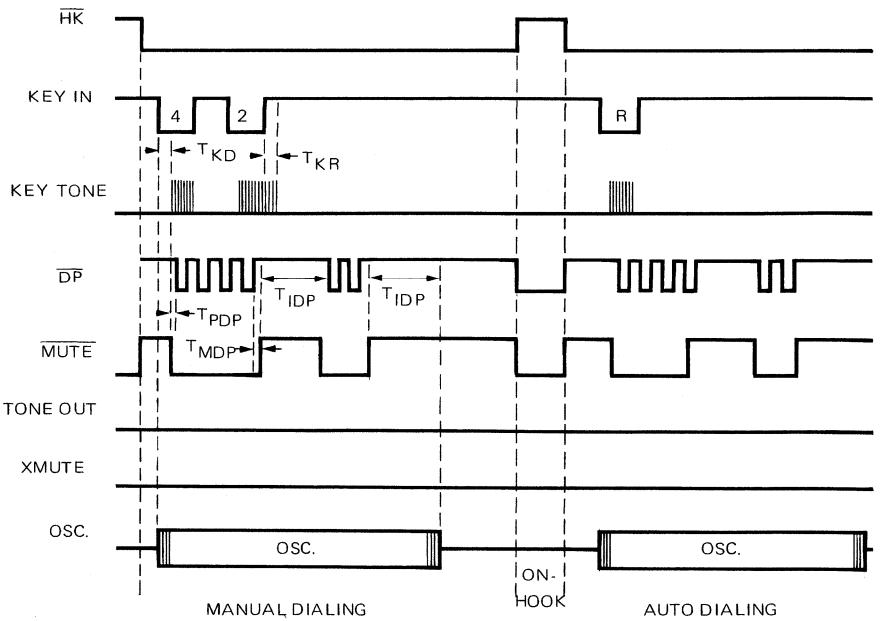
G. Long distance service memory dialing

The UM91265 provides a special memory location for storing a long distance service company access code. It also provides an automatic switching function which changes from Pulse mode to Tone mode after a pause. This function makes it easier for a subscriber to use a long distance service company (such as MCI or SPRINT) without confusing the Pulse/Tone switching operation.

1. Storing the long distance service company code, to LDC memory.
   S, DxDxDx . . . , P, P, DxDxDx . . . S, LDC
   Two Pause Authorized Access codes.
2. LDC dialing
   0−0 ↑, LDC, ZiZiZi 0−0 ↓
   Note: The chip will automatically switch to tone mode after the two pause duration (6.2ms) even if the Authorized Access Codes you Store are pulse codes.

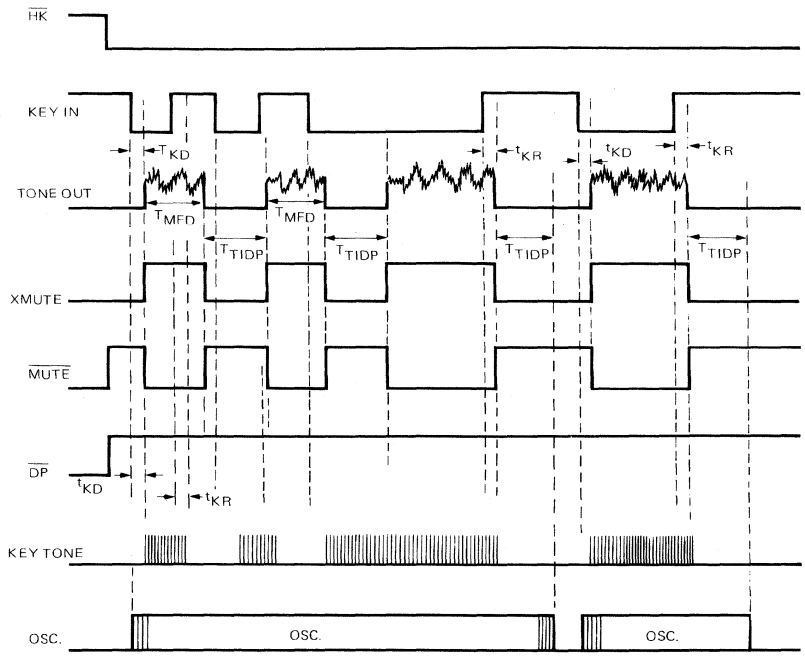
Timing Waveforms

(1) PULSE MODE TIMING

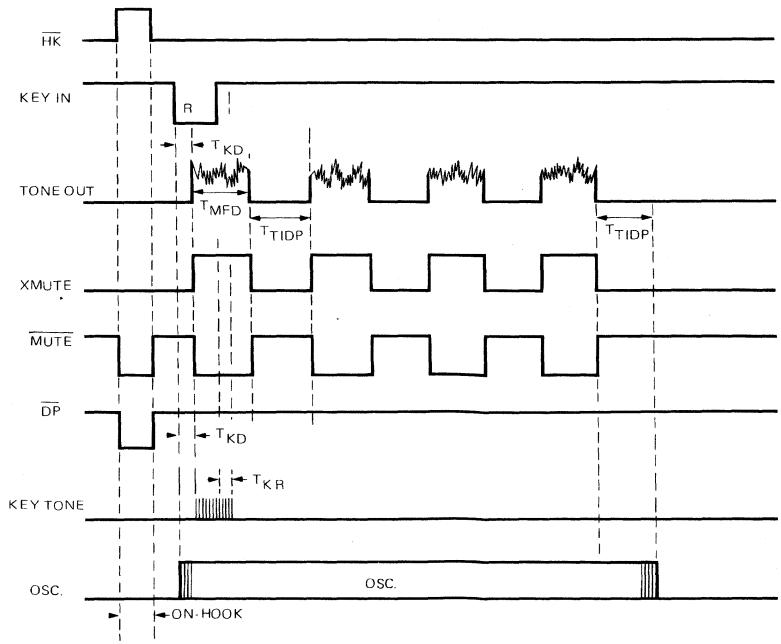


(2) TONE MODE TIMING

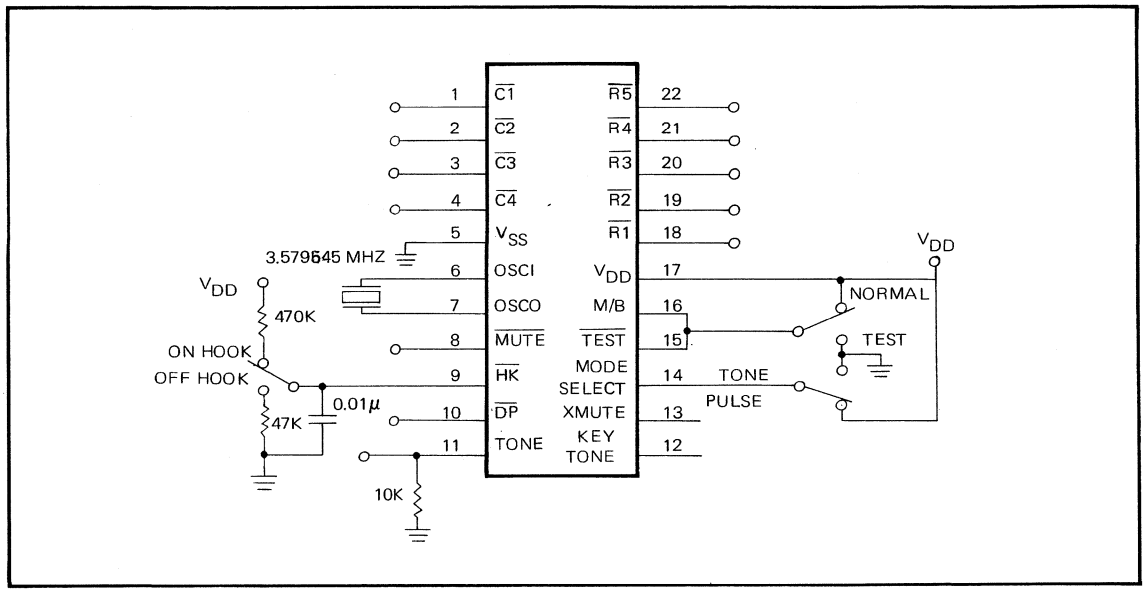
(a) NORMAL



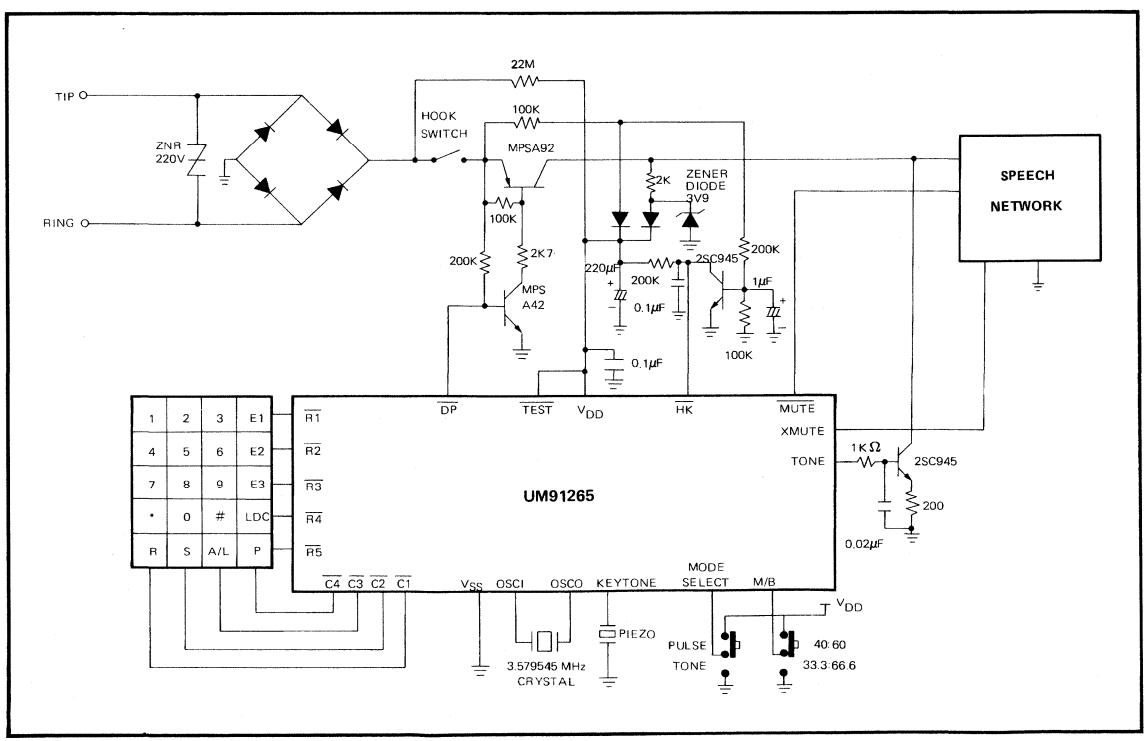
(b) REDIALING



Typical Application Circuit

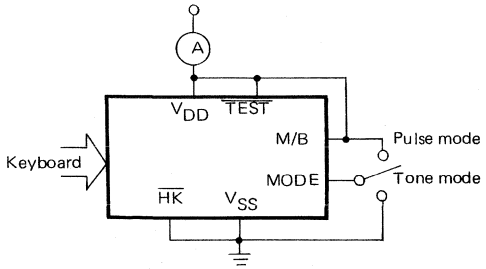


Typical Application Circuit

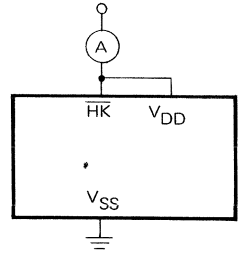


Test Circuits

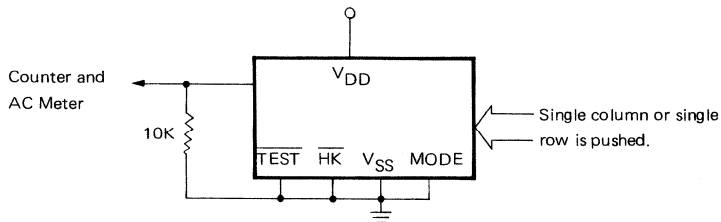
1.



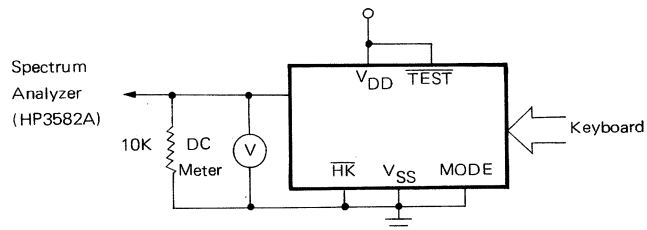
2.



3.



4.



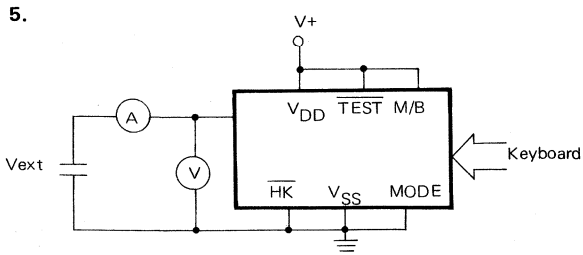
$$DIST_{db} = 20 \log \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (Vn)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

* $V_1 \ldots . V_n$ are extraneous frequency (i. e. intermodulation and harmonic) components in the 500HZ to 3400HZ band.

* V_L, V_H are the individual frequency components of the DTMF signal.

Note: Whether keyboard is pushed, refer to the DTMF mode timing diagram.

5.



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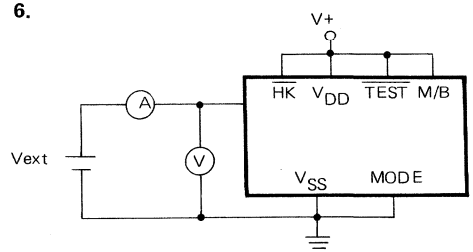
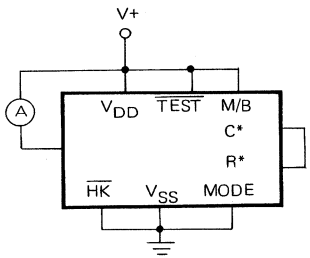


Note: Whether keyboard is pushed, refer to the DTMF mode timing diagram.

7.



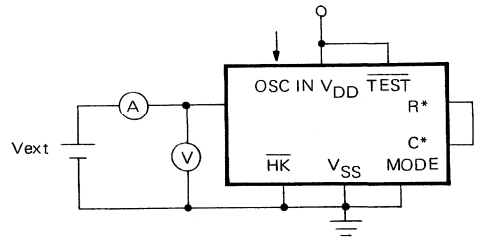
R*: any row of R1 - R5

C*: any column of C1 - C4

Isink = I/(1 - Duty Cycle)

I is the net dc current.

8.



Procedure:

1 Provide clocks until output changes to high.

2 Test the current.

Note: $\overline{TEST}$ pin can be combined with V_{SS} in order to speed up testing.

UMC

UM91270

20 Memory Tone/Pulse Dialer

Features:

- 32-digit redial memory (31 digits in tone mode).
- Twenty 18-digit number memories (17 digits in tone mode) with direct access keys.
- Tone/pulse mode switching: tone capability available in pulse mode through use of the "T" (pulse to tone) key.
- Low operating voltage: 1.8 to 5.0 V in pulse mode
  2.5 to 5.0 V in tone mode.
- Can be used with 480 KHz ceramic resonator.
- Selectable make/break ratio.
- Selectable dialing rate.
- Flash can be stored in digit form; 0.6 second flash, 1.6 second pause.
- Page mode: M1 to M10 first page, M11 to M20 second page.
- 100 ms minimum tone output duration.
  100 ms minimum interdigit pause.
- 4.0 second access pause.
- Memory transfer from number to redial memory in dialing mode.
- Allows overflow in normal dialing.

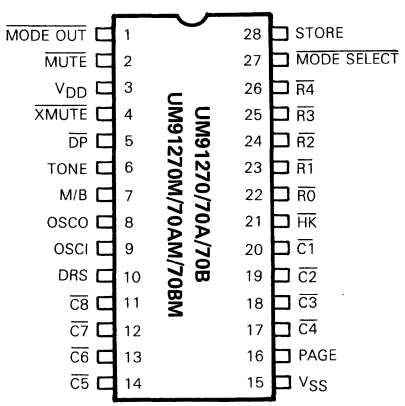
General Description

The UM91270 is a switchable tone/pulse dialer with twenty 18-digit number memories and a 32-digit redial memory. Pulse to tone mode switching can be performed either by using a slide switch or by depressing the tone key. UMC's HCMOS-2B technology has been used to produce this device, resulting in low power requirements, high noise immunity, and easy interfacing with a variety of telephones.

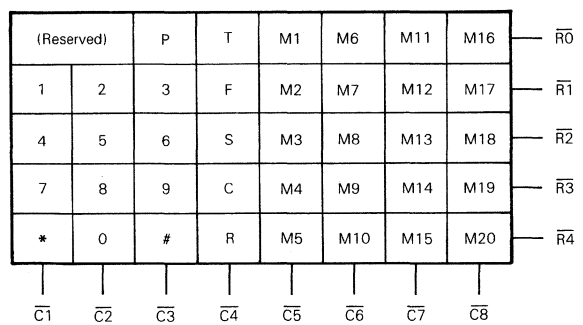
Ordering Information

Part No.	Access Pause	Flash	Package
UM91270	4 s	600 ms	P-DIP 28L
UM91270A	4 s	100 ms	
UM91270B	2 s	600 ms	
UM91270M	4 s	600 ms	SO 28L
UM91270AM	4 s	100 ms	
UM91270BM	2 s	600 ms	

Pin Configuration

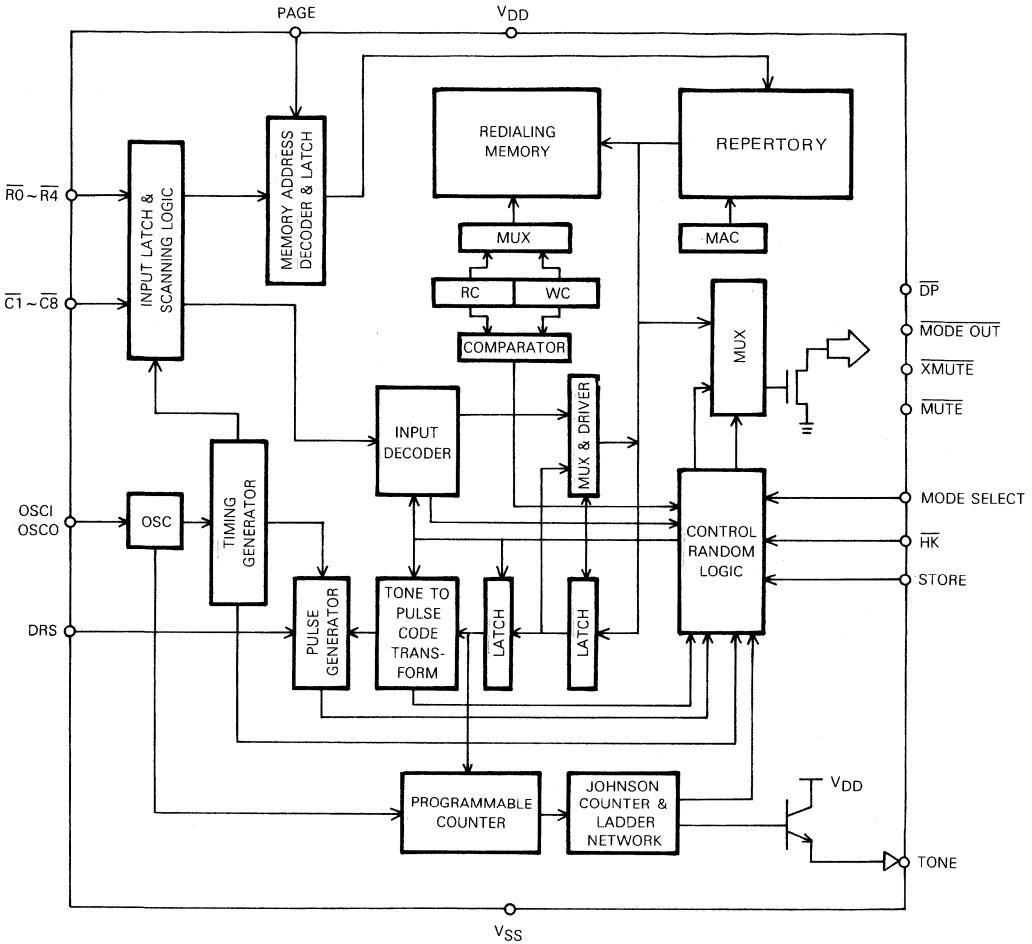


Keyboard Assignment



P: Pause
T: Pulse to Tone Key
F: Flash
S: Store
C: Clear
R: Redial

Block Diagram



Absolute Maximum Ratings *

Power supply voltage ($V_{DD}-V_{SS}$)..... −0.3V to +6.0V
Input voltage (V_{IN})..... −0.3 to V_{DD} + 0.3V
Maximum power dissipation (at 25°C).....600 mW
Operating temperature (T_{OP})..... −20°C to +70°C
Storage temperature (T_{STG})..... −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the sections of this specification listing dealing with operational procedures is not implied.

DC Characteristics

(V_{DD} = 3.5 V, V_{SS} = O. V, F_{OSC} = 480 KHz, T_{OP} = 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test CKT.
Operating Voltage	V_{DD}	Pulse mode	1.8		5.0	V	A
		DTMF mode	2.5		5.0		
Memory Retention Voltage	V_{MR}		1.0			V	
Memory Retention Current	I_{MR}	$V_{DD}=\overline{HK}=1$ V all outputs unloaded		0.05	0.1	μA	
Standby Current	I_{SD}	$\overline{HK}=V_{SS}$ all outputs unloaded		5	50	μA	A
Supply Operating current	I_{DDP}	oscillator running		0.16	0.5	mA	A
	I_{DDT}	all outputs unloaded		0.4	1.0	mA	
Output Sink Current $\overline{DP}$ $\overline{MUTE}$ $\overline{XMUTE}$	I_{OL1}	V_{OL} = 0.4 V	1.0	10		mA	B
	I_{OL2}	V_{OL} = 0.4V, V_{DD} = 2.0 V	0.4	5		mA	B
Output Sink Current $\overline{MODE}$ $\overline{OUT}$	I_{OL1}	V_{OL} = 0.4 V	3.0	10		mA	B
	I_{OL2}	V_{OL} = 0.4, V_{DD} = 2.0 V	1.0	6		mA	B
Input voltage Range	V_{IH}		$0.8V_{DD}$		V_{DD}	V_{DD}	
	V_{IL}		0.		$0.2V_{DD}$	V_{DD}	
Row Input Current	I_R	$V_{IN}=3.5$V, all outputs unloaded	1	4	60	μA	C
Column Input Current	I_C	$V_{IN}=0$V, all outputs unloaded	70	250	800	μA	C
Single Row Tone Output Amplitude	V_{OR}	Rload = 10KΩ, $V_{DD}=2.5$V	500	540	580	mVp-p	D
	V_{OR}	Rload = 10KΩ, $V_{DD}=5.0$V	510	560	600	mVp-p	D
Single Column Tone Output Amplitude	V_{OC}	Rload = 10KΩ, $V_{DD}=2.5$V	620	680	730	mVp-p	D
	V_{OC}	Rload = 10KΩ, $V_{DD}=5.0$V	650	710	760	mVp-p	D
Pre-emphasis	Twist		1	2	3	dB	D
Valley of Single Tone	V_V			V_{DD}-1.8	V_{DD}-1.6	V	sec
Distortion	DIS %	*(see note below)		1	5	%	D

*Note:

$$DIS\ (\%) = \frac{100\ (V1^2 + V2^2 + \ldots.. + Vn^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$$

where

a) V1....Vn are the intermodulation or harmonic frequencies in the 500 Hz to 3400 Hz band, and
b) V_{IL} and V_{IH} are the individual frequency components of the DTMF signal.

Tone/Pulse Dialer

AC Characteristics

(V_{DD} = 3.5 V, Vss = 0. V, F_{OSC} = 480 KHz, T_{OP} = 25°C unless otherwise specified.)

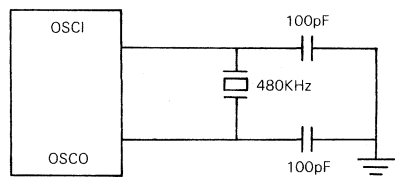
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PULSE						
Make/Break Ratio	M/B	M/B = V_{DD}		1/2		
		M/B = V_{SS}		2/3		
Dial Pulse Rate	DR	DRS = V_{DD}		20		PPS
		DRS = V_{SS}		10		
Make Time	T_M	10 PPS M/B = 1/2		33.3		ms
		10 PPS M/B = 2/3		40		
		20 PPS M/B = 1/2		16.7		
		20 PPS M/B = 2/3		20		
Break Time	T_B	10 PPS M/B = 1/2		66.7		ms
		10 PPS M/B = 2/3		60		
		20 PPS M/B = 1/2		33.3		
		20 PPS M/B = 2/3		30		
Inter-digit Pause Time	T_{IDP}	10 PPS M/B = 1/2		827		ms
		10 PPS M/B = 2/3		820		
		20 PPS M/B = 1/2		603		
		20 PPS M/B = 2/3		600		
Pre-digit Pause Time	T_{PDP}	10 PPS M/B = 1/2		830		ms
		10 PPS M/B = 2/3		830		
		20 PPS M/B = 1/2		620		
		20 PPS M/B = 2/3		620		
$\overline{MUTE}$, $\overline{DELAY}$, $\overline{XMUTE}$ Time	T_{MDP}	10 PPS M/B = 1/2		33.3		ms
		10 PPS M/B = 2/3		40		
		20 PPS M/B = 1/2		16.7		
		20 PPS M/B = 2/3		20		
TONE						
Minimum tone duration	T_{MFD}			100		ms
Minimum Tone Inter-digit Pause Time	T_{TIDP}			100		ms
Tone Output Pre-digit Pause Time	T_{RPDP}			0.		ms
$\overline{XMUTE}$ Delay Time	T_{MDP}			100		ms
Access Pause Time	T_{AP}			4.26/2		sec
Oscillator Start-up Time	T_{START}			10		ms
$\overline{MUTE}$, $\overline{XMUTE}$ Start-up Time	T_{MS}			28		ms
Keypad Debounce Time	T_{KD}			17		ms
Key Scan Frequency	F_{KS}	$\overline{R1} \sim \overline{R5}$, $\overline{C1} \sim \overline{C8}$		300		Hz
Flash Time	T_{FLASH}			600/100		ms
Pause Post Flash Time	T_{PPF}			1.6		sec

R/C	Conditions	Spec.	Actual	Error(%)	Unit
$\overline{R1}$	F_{OSC} = 480 KHz	697	695.65	− 0.19	Hz
$\overline{R2}$		770	769.23	−0.1	Hz
$\overline{R3}$		852	851.06	−0.11	Hz
$\overline{R4}$		941	941.18	+0.02	Hz
$\overline{C1}$		1209	1212.12	+0.26	Hz
$\overline{C2}$		1336	1333.33	−0.2	Hz
$\overline{C3}$		1477	1481.48	+0.3	Hz

Pin Description

Pin	Designation	Description
11—14 17—20 22—26	$\overline{R0}$ ~ $\overline{R4}$ $\overline{C1}$ ~ $\overline{C8}$	Key inputs. A key operation is activated when the row and column corresponding to a particular key are connected. When the $\overline{HK}$ pin is at V_{DD} level (see below), all row and column pins are in the high state and are at high impedance. When a key is depressed, the column input for that key is pulled high and the row output is pulled low; a scanning signal is present on the other row and column pins. Typical keyboard input debounce time is 22 ms.
21	$\overline{HK}$	Hook switch input. $\overline{HK}$ = V_{DD}: on-hook state (device inactive). $\overline{HK}$ = V_{SS}: off-hook state (device activated).
7	M/B	Dial pulse make/break ratio select input. M/B pin = V_{DD}: make/break ratio = 1:2 M/B pin = V_{SS}: make/break ratio = 2:3
10	DRS	Dialing rate select input. DRS = V_{DD}: dialing rate = 20 PPS DRS = V_{SS}: dialing rate = 10 PPS
1	$\overline{MODE\ OUT}$	Mode output. N-channel open drain output. Output transistor is switched off in the on-hook state and when the dial pulse output mode is activated; switched on at all other times.
2	$\overline{MUTE}$	Mute output. N-channel open drain output. Output transistor is switched on during pulse dialing sequence; switched off at all other times.
4	$\overline{XMUTE}$	Transmit mute output. N-channel open drain output. Output transistor is switched on during dialing sequence (both pulse and tone modes) and off at all other times.

Pin Description (Continued)

Pin	Designation	Description
3 15	V_{DD} V_{SS}	Positive power supply input (operating range 1.8 to 5.0 V). Negative power input.
5	$\overline{DP}$	Dial pulse output. N-channel open drain output. When in off-hook pulse mode, output is low during dial pulse "break" and "flash" operations. Output is "open" at all other times. The UM91270 provides an 820 ms IDP (inter-digit pause) when set at the 10 pps dial pulse rate and a 600 ms IDP when set at the 20 pps dial pulse rate.
6	TONE	DTMF signal output. Bipolar structure output. Typical equivalent output impedance: 1.5 KΩ Both normal dialing and redialing minimum tone and IDP durations are built-in.
8 9	OSCO OSCI	Oscillator circuit output and input. Complete oscillator circuit is formed by adding one 480 KHz ceramic resonator, two 100 PF serial loading capacitors across the oscillator output and input pins. Oscillator circuit is activated when the HK pin is low: When V_{DD} = 3.0 V, typical oscillator start-up time is 10 ms. 
16	PAGE	Page select input for reduced keyboard application. When input level to this pin = V_{SS}, the M1 to M20 keys correspond directly to the 20 repertory memories. When input level to this pin = V_{DD}, the M11 to M20 repertory memory locations replace the M1 to M10 memories on the M1 to M10 keys.
27	$\overline{\text{MODE SELECT}}$	Tone/pulse mode select input. When mode select input = V_{DD}, pulse mode is activated. When mode select input = V_{SS}, tone mode is activated. During a pulse dialing sequence, switching this input from V_{DD} to V_{SS} will cause the UM91270 to insert a tone code and a pause code into its buffer memory automatically, then change the remaining digits entered to a tone signal. Once tone mode has been selected, changing the mode select input from V_{SS} to V_{DD} will not switch the UM91270 back to pulse mode again except by means of an on-hook operation. Pressing the first digit after the off-hook operation during tone mode causes two codes to be written into the buffer memory: the first is a tone code, the second a digit code.
28	STORE	Store mode switch control. Off-hook store mode is activated when store pin input = V_{DD}. When off-hook store mode has been activated, the UM91270 will not return to normal mode again until the store pin input level is changed from V_{DD} to V_{SS}. On-hook store mode is obtained via application circuits. This input level is directly related to the HOOK pin input via an application circuit.

Operational Procedures

Symbol Definitions:

Dp = pulse digit (0 through 9).
Dt = tone digit (0 through 9, *, #).
Dg = pulse digit or tone digit.
Mj = memory location (M1, M2, M3 .....M20).
ZiZiZi = conversation mode.
O-O↑ = off-hook.
O-O↓ = on-hook.
⎍ = input level from low to high.
⎍ = input level from high to low.

Recommended Operations:

* Normal dialing in tone mode:
  O-O↑; Dp.....Dp; ZiZiZi; O-O↓.
* Normal dialing in pulse mode:
  O-O↑; Dt.....Dt; ZiZiZi; O-O↓.
* Normal dialing in pulse to tone mode via the [T] key:
  (T/P input hold on Vss level) O-O↑; Dp.....Dp; [T] ; Dt.....Dt; ZiZiZi; O-O↓.
* Normal dialing in pulse to tone mode via T/P input:
  O-O↑; Dp.....Dp; T/P⎍; Dt.....Dt; ZiZiZi; O-O↓.
  (Note: In normal dialing mode, digits will be dialed out exactly if the total number of digits to be dialed is less than 32.)
* Redialing:
  O-O↑; [R] ; ZiZiZi; O-O↓.
  (Note: this operation activates the UM91270 to dial out the number contained in the buffer memory.)
* Repertory dialing for one number memory:
  O-O↑; Mj; ZiZiZi; O-O↓.
* Repertory dialing for cascaded memory:
  O-O↑; Mj.....Mj; ZiZiZi; O-O↓.
  (Warning: No more than 32 digits should be entered into the cascaded memory. Overflow digits will be truncated and will not be dialed out.)
* Clearing buffer memory:
  O-O↑; [C] .
* Clearing number memories via the [S] key:
  O-O↑; [S] ; [C] ; Mj; (return to normal mode).
* Clearing number memories via the store switch/ [C] key:
  O-O↑; store switch ⎍; [C] , Mj, [C] , Mj .....; store switch ⎍ (return to normal mode).
  (Note: The store switch input will latch the UM91270 in the store mode unless the store switch is switched back to the normal mode.)
* Storing numbers to memories via the [S] key:
  O-O↑; [S] ; Dg...Dg; Mj; [S] Dg...Dg; Mj... (return to normal mode).
* Storing numbers to memories via the store switch:
  O-O↑; store switch ⎍; Dg....Dg; Mj; Dg....Dg; Mj; ....; store switch ⎍ (return to normal mode).
* Clearing input errors:
  .....Dgx,....Dgx; [C] ; Dg.....Dg; Mj;..... (erroneous input digits Dgx will not be stored into the Mj repertory memory address).

Functional Description

N-channel open drain output-$\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$, $\overline{MODE}$ $\overline{OUT}$

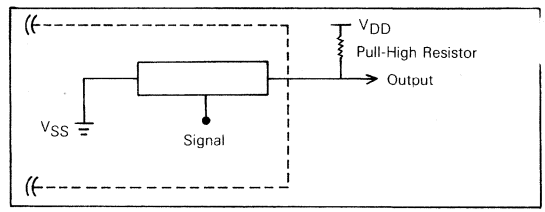


Figure 1.

DTMF Generator

The UM91270 has a well-designed DTMF output structure, with a 6 level, 12 segment stable reference voltage and a fixed output amplitude. This generator consists of a reference voltage regulator and a bipolar emitter follower that provides a V_{DD}–1.8 V reference voltage and an approximately 1.2 V tone output swing.

The UM91270's THD (total harmonic distortion) is 5% maximum when used under recommended conditions (V_{DD} = 1.8 V to 5.0 V, frequency between 500 and 3400 Hz).

The DTMF output signal (figure 2) and its output characteristics are shown in figures 3 and 4, "DTMF Signal THD vs. Operating Voltage" and "DTMF Output Amplitude vs. Operating Voltage"

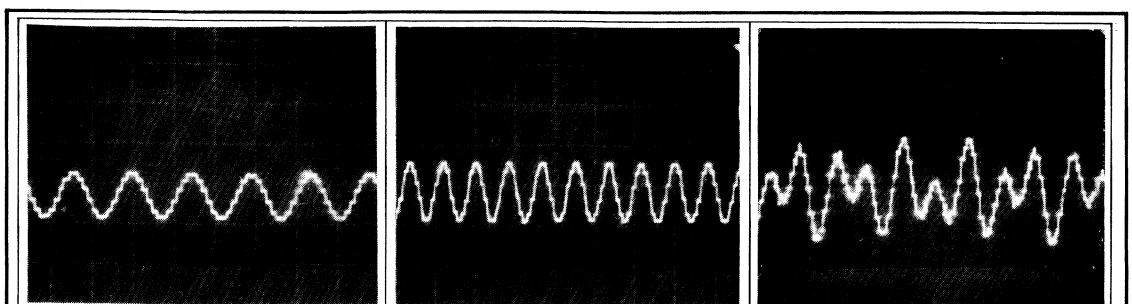
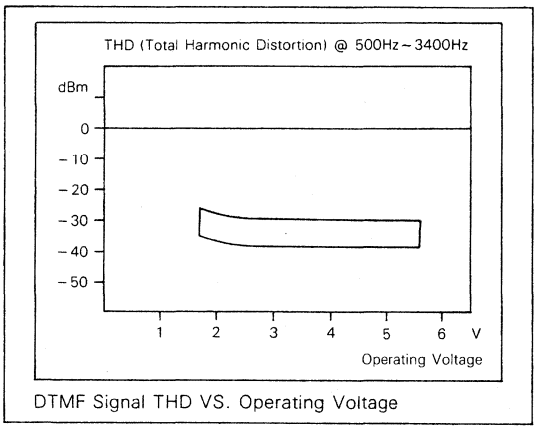
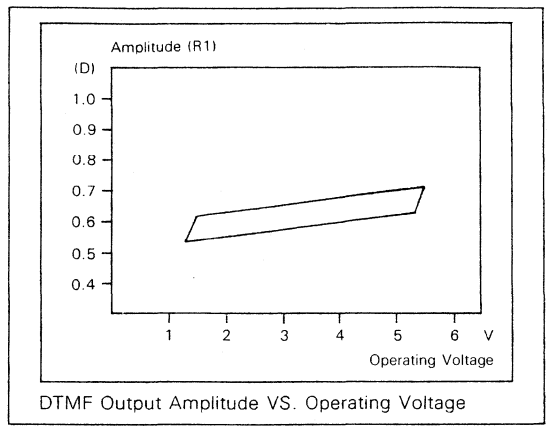


Figure 2. Waveforms



DTMF Signal THD VS. Operating Voltage

Figure 3.

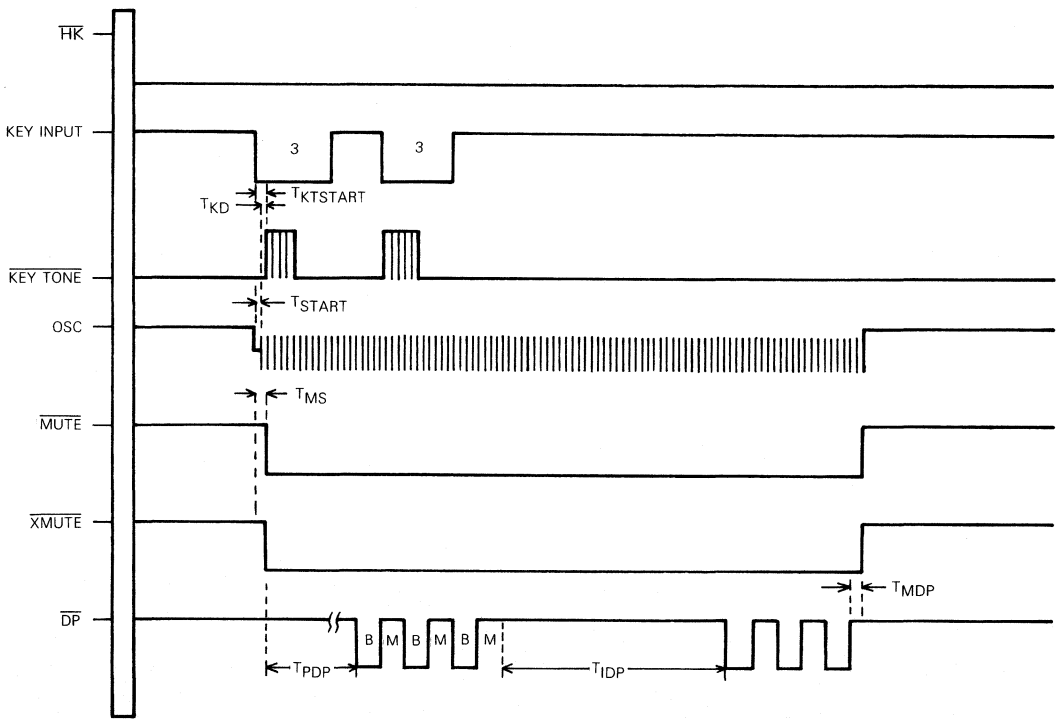


DTMF Output Amplitude VS. Operating Voltage

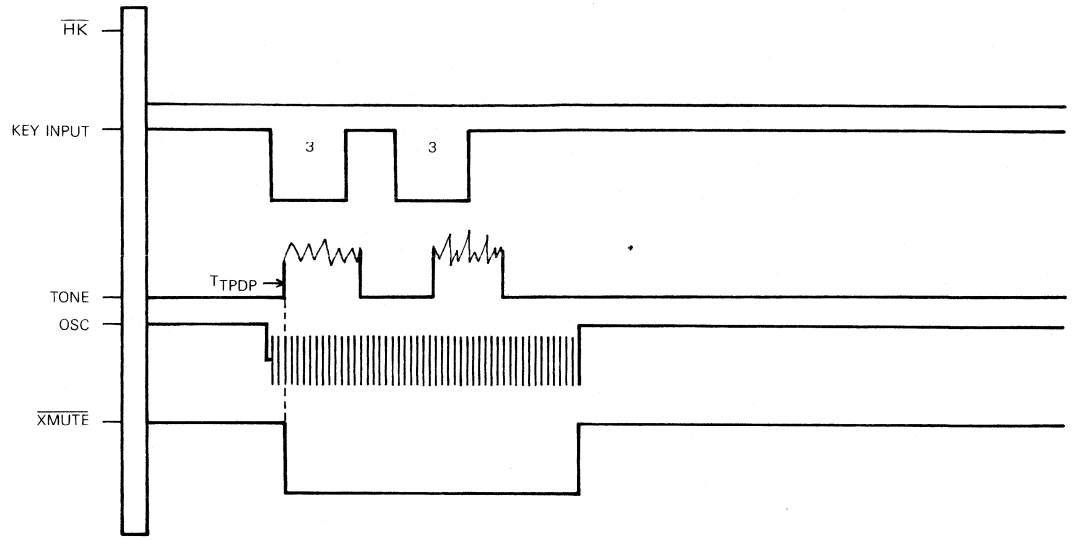
Figure 4.

Timing Diagrams

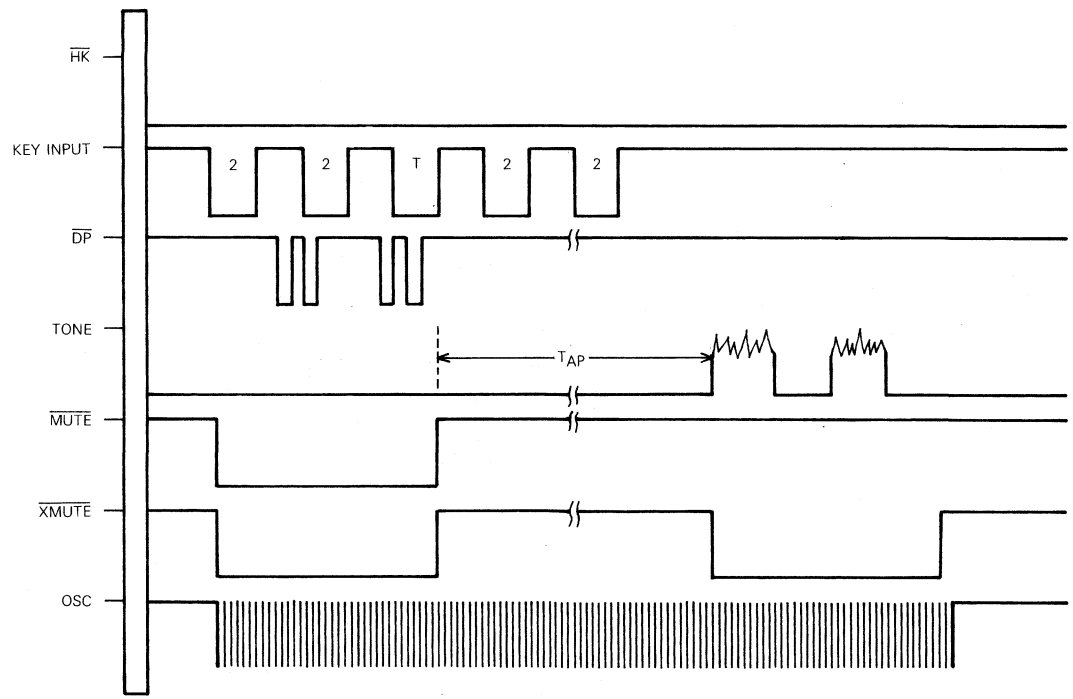
PULSE MODE TIMING DIAGRAM



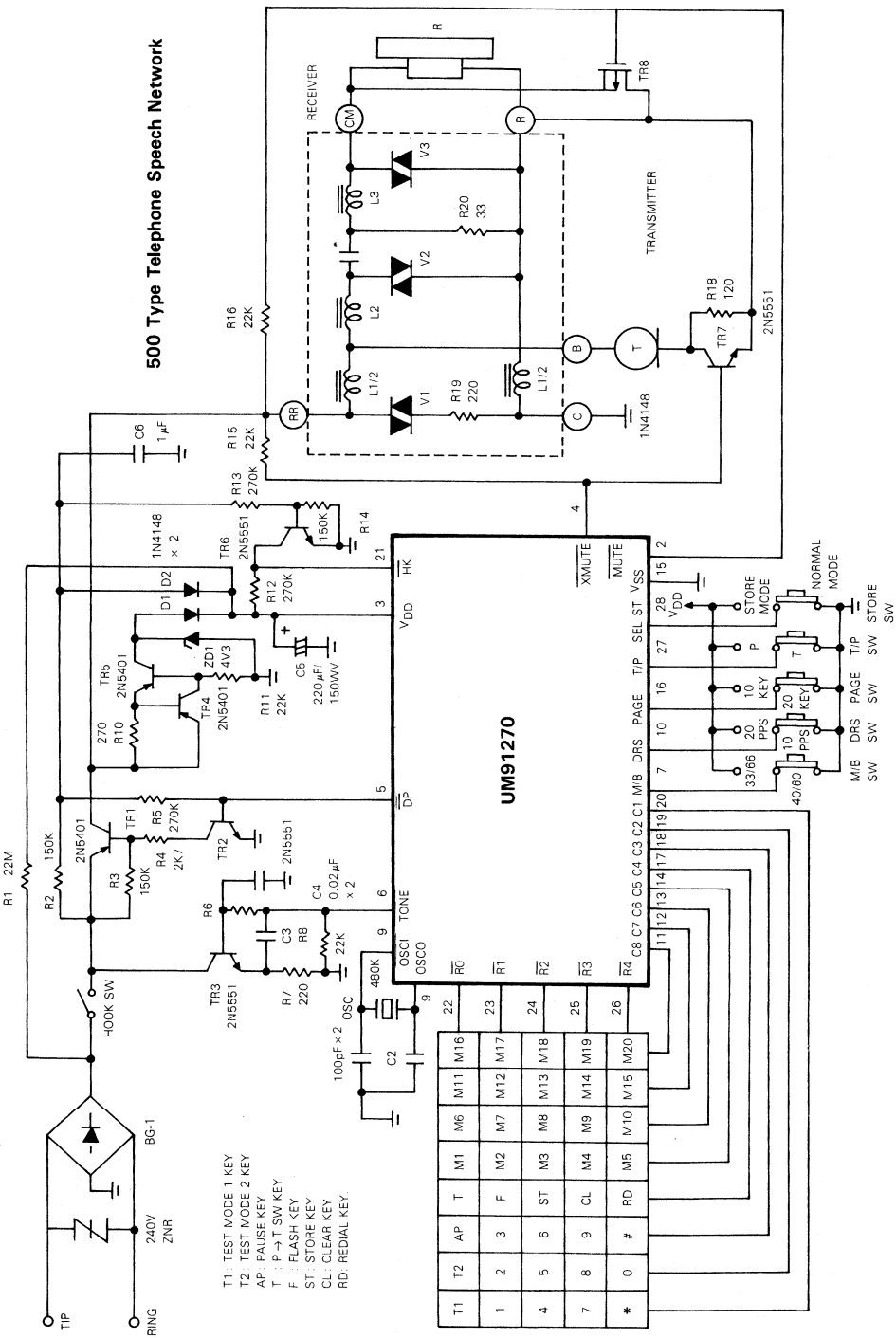
TONE MODE TIMING DIAGRAM



NORMAL PULSE TO TONE MIXED DIALING VIA [T] KEY

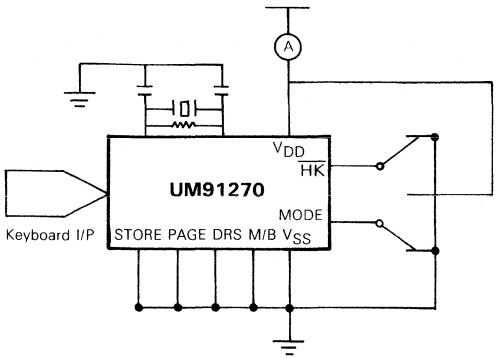


Typical Application Circuit

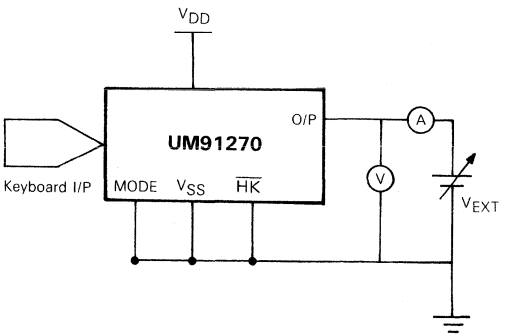


Test Circuits

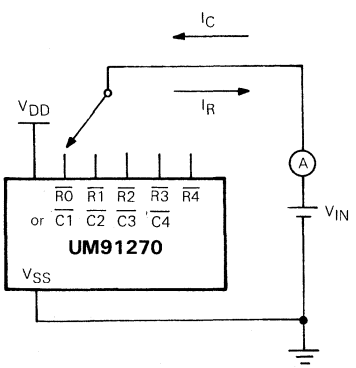
(A)



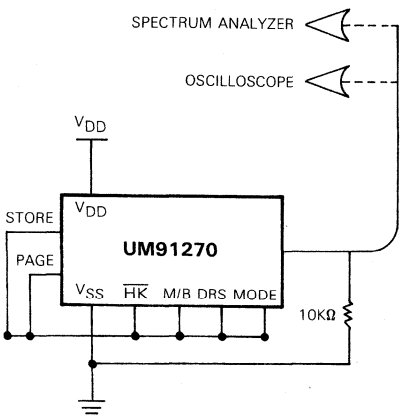
(B)



(C)



(D)



* OSCILLOSCOPE: TEKTRONIX 468
* SPECTRUM ANALYZER: HP 3585A

Tone/Pulse Dialer

UM91271/72

20 Memory Tone/Pulse Dialer

Features

- 32-digit redial memory
- 20 16-digit repertory memories
- Repertory dialing accessible by direct or indirect key-in
- Unlimited cascaded dialing from repertory memories for numbers greater than 16 digits
- 1.0 sec auto-access pause for repertory dialing when switching from pulse to tone mode
- Key-tone function provided for pulse mode, function keys, and repertory memory keys
- Flash function can be stored in memory; flash duration 600 msec
- Oscillator circuit for 480 KHz ceramic resonator provided on-chip

General Description

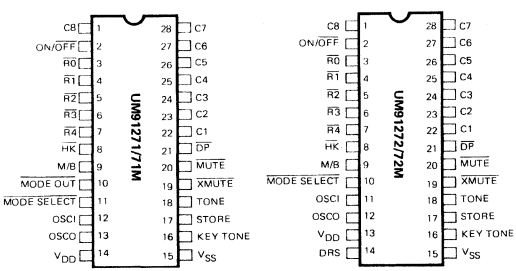
The products in the UM91271 series are tone/pulse dialers, each featuring 20 16-digit number memories and a 32-digit redial memory. Repertory dialing can be accessed by direct or indirect operation, and cascaded dialing is allowed for stored numbers longer than 16 digits. On-hook or off-hook number storing functions are pin selectable. Other features include Flash and Pause keys in redial mode.

Note: The 32 digits of redial memory and 16 digits of repertory memory mentioned above are available in pulse mode. When dialing in Tone mode, one digit of memory will be occupied by the tone code, which reduces the total numbers of digits available in tone mode to 31 and 15 respectively.

Ordering Information

Part No.	Dialing Rate	Package
UM91271	10 pps	P-DIP
UM91272	10/20 pps	P-DIP
UM91271M	10 pps	SO
UM91272M	10/20 pps	SO

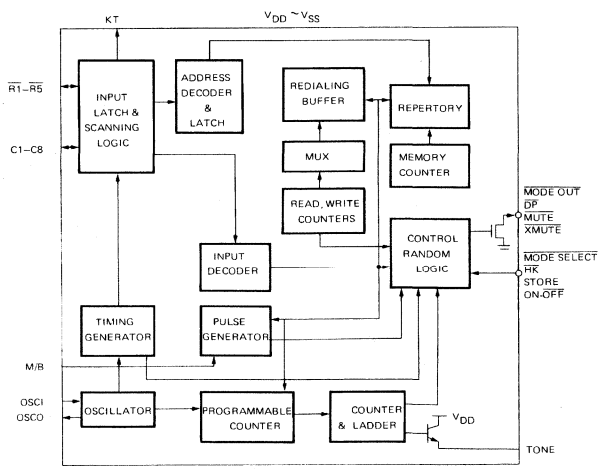
Pin Configurations and Keyboard Assignments



TEST1	STORE	TEST2	T	M1	M6	M11	M16	R0
1	2	3	F	M2	M7	M12	M17	R1
4	5	6	A/L	M3	M8	M13	M18	R2
7	8	9		M4	M9	M14	M19	R3
*	0	#	R/P	M5	M10	M15	M20	R4
C1	C2	C3	C4	C5	C6	C7	C8	

T: Pulse to DTMF
F: Flash
A/L: Auto/Location
R/P: Redial/Pause

Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage (V_{DD}, V_{SS}) ..... −0.6V to 5.5V
Input Voltage (V_{IN}) ..... −0.3V to V_{DD}+0.3V
Maximum Power Dissipation (at 25°C) 600mW
Operating Temperature (T_{OP}) ..... −20°C to +70°C
Storage Temperature (T_{STG}) ..... −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 480 KHz, T_{OP} = 25°C unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD}	1.8		5.0	V	Pulse Mode	A
		2.0		5.0		DTMF Mode	A
Memory Retention Voltage	V_{MR}	1.0			V		
Memory Retention Current	I_{MR}		0.05	0.5	μA	V_{DD} = 1.0V, $\overline{HK}$ = V_{DD} All outputs unloaded	
Supply Operating Current	I_{DDP}		0.35	0.5	mA	Oscillator running	A
	I_{DPT}		0.50	1.0		Outputs unloaded	
Standby Current	I_{SD}			0.5	μA	$\overline{HK}$ = V_{DD}	A
				50		$\overline{HK}$ = V_{SS} No key-in	
Output Sink Current: $\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$, $\overline{MODE\ OUT}$	I_{OL1}	1.0			mA	V_{OL} = 0.4V, V_{DD} = 2V	B
	I_{OL2}	3.0			mA	V_{OL} = 0.4V, V_{DD} = 3.5V	
Output Sink/Drive Current Key Tone	I_{OL3}	0.5			mA	V_{OL} = 0.4V	B
	I_{OHI}	0.5			mA	V_{OH} = V_{DD} − 0.4V	
Input Voltage	V_{IL}	0		0.2	V_{DD}		
	V_{IH}	0.8		1.0			
Keyboard Input Current	Column	70	250	800	μA	All outputs unloaded	C
	Row	1	4	60	μA		
Single Row Tone Output Amplitude	V_{OR}	510	560	590	mV_{P-P}	R_{LOAD} = 10KΩ, V_{DD} = 2.5V	D
		520	580	610		R_{LOAD} = 10KΩ, V_{DD} = 5.0V	
Single Col. Tone Output Amplitude	V_{OC}	640	700	740	mV_{P-P}	R_{LOAD} = 10KΩ, V_{DD} = 2.5V	D
		680	730	770		R_{LOAD} = 10KΩ, V_{DD} = 5.0V	
Pre-Emphasis	Twist	1	2	3	dB		D
Valley of Single Tone	V_V		V_{DD}−1.8	V_{DD}−1.6	V_{DD}		D
Distortion	DIS%		1	5	%	Note 1	D

Note 1: $DIS\% = \dfrac{100(V_1^2 + V_2^2 + \ldots V_n^2)^{1/2}}{(V_L^2 + V_H^2)^{1/2}}$

1. $V_1 \ldots V_n$ are the intermodulation or harmonic frequencies in the 500 Hz to 3400 Hz band.
2. V_L, V_H are the individual frequency components of the DTMF signal.

AC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 480 KHz, T_{OP} = 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
PULSE							
Make/Break Ratio	M/B	M/B = V_{DD}			1/2		
		M/B = V_{SS}			2/3		
Dial Pulse Rate	DR	UM91271			10		pps
		UM91272			10/20		
Make Time	T_M	10 pps	M/B = 1/2		33.3		ms
			M/B = 2/3		40		
		20 pps	M/B = 1/2		16.7		
			M/B = 2/3		20		
Break Time	T_B	10 pps	M/B = 1/2		66.7		ms
			M/B = 2/3		60		
		20 pps	M/B = 1/2		33.3		
			M/B = 2/3		30		
Inter-digit Pause	T_{IDP}	10 pps	M/B = 1/2		836		ms
			M/B = 2/3		830		
		20 pps	M/B = 1/2		613		
			M/B = 2/3		610		
Pre-digit Pause	T_{PDP}	10 pps	M/B = 1/2		820		ms
			M/B = 2/3		820		
		20 pps	M/B = 1/2		612		
			M/B = 2/3		612		
$\overline{MUTE}$, $\overline{XMUTE}$ Delay Time	T_{MDP}	10 pps	M/B = 1/2		33.3		ms
			M/B = 2/3		40		
		20 pps	M/B = 1/2		16.7		
			M/B = 2/3		20		
TONE							
Minimum Tone Duration	T_{MFD}				100		ms
Minimum Tone Inter-digit Pause	T_{TIDP}				100		ms
Tone Output Pre-digit Pause	T_{TPDP}				0		ms
$\overline{XMUTE}$ Delay Time	T_{MDT}				100		ms
Auto access Pause	T_{AP}				1.0		S
Oscillator Startup Time	T_S				10		ms
$\overline{XMUTE}$, $\overline{MUTE}$ Startup Time	T_{MS}				22		ms
Keypad Debounce Time	T_{KD}				20		ms
Key Scan Frequency	F_{KS}	$\overline{R1}$ to $\overline{R5}$, C1 to C8			300		Hz
Key Tone Frequency	F_{KT}				1.2		KHz
Key Tone Duration	T_{KT}				42		ms
Key Tone Startup Time	$T_{KTSTART}$				20		ms
Flash Time	T_F				600		ms
Pause Time	T_P				2		S

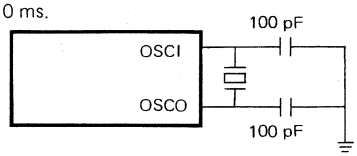
AC Characteristics (Continued)

Parameter	Symbol	Condition	Spec.	Actual	Error (%)	Unit
DTMF Row Frequency	$\overline{R1}$	F_{OSC} = 480 KHz	697	695.65	−0.19	Hz
	$\overline{R2}$		770	769.23	−0.10	
	$\overline{R3}$		852	851.06	−0.11	
	$\overline{R4}$		941	941.18	+0.02	
DTMF Column Frequency	C1		1,209	1,212.12	+0.26	
	C2		1,336	1,333.33	−0.20	
	C3		1,477	1,481.48	+0.30	

Pin Description

Pin		Designation	Description
91271	91272		
3 4 5 6 7 22 23 24 25 26 27 28 1	3 4 5 6 7 22 23 24 25 26 27 28 1	$\overline{R0} \sim \overline{R4}$ C1 ~ C8	Key inputs. Key operations are activated when the row and column corresponding to a particular key are connected. When the on/off input is low, i. e., on-hook store mode is inhibited, both the row and column inputs are low during the on-hook state. When the on/off input is high, i. e., the on-hook store mode is available, the column inputs are pulled high and the row inputs low. A scanning signal is present on both row and column pins under valid key-in conditions. Typical key-in debounce time is 22 ms.
2	2	ON/$\overline{OFF}$	On-Hook/Off-Hook store mode selection input. On/Off = V_{DD}: On-hook store mode. On/Off = V_{SS}: Off-hook store mode.
8	8	$\overline{HK}$	Hook switch input. $\overline{HK}$ = V_{DD}: On-hook state. $\overline{HK}$ = V_{SS}: Off-hook state.
9	9	M/B	Make/Break ratio select input. M/B = V_{DD}: M/B ratio = 1/2. M/B = V_{SS}: M/B ratio = 2/3.
10		$\overline{MODE\ OUT}$	Mode output. This is an N-channel open drain output. The output transistor is switched on and pulled low during tone mode operation.

Pin Description (Continued)

Pin		Designation	Description
91271	91272		
11	10	$\overline{\text{MODE SELECT}}$	Pulse/Tone mode select input. Mode Select = V_{DD} : pulse mode activated. Mode Select = V_{SS} : tone mode activated.
12 13	11 12	OSCI OSCO	Oscillator Input/Output. Complete oscillator circuit consists of a 480 KHz ceramic resonator, two 100 pF serial loading capacitors, and a 470 KΩ feedback resistor is built in. Oscillator circuit is activated when a valid key-in occurs; typical start-up time is 10 ms. 
14	13	V_{DD}	Positive power supply input.
	14	DRS	Dialing rate select input. DRS = V_{DD} : dialing rate = 20 pps. DRS = V_{SS} : dialing rate = 10 pps.
15	15	V_{SS}	Negative power supply input.
16	16	KEY TONE	Key-in tone output. The Key-in tone output is intended to serve as a valid key-entry indicator. This output is activated when function keys are depressed and during pulse mode; it adopts an inverter output structure and is able to drive a piezo directly.
17	17	STORE	Store switch input. Store = V_{DD} : store mode. Store = V_{SS} : normal mode.
18	18	TONE	DTMF signal output. A built-in fixed voltage reference circuit provides a constant tone output level.
19	19	$\overline{\text{XMUTE}}$	Transmit mute output. N-channel open drain output. Output transistor is switched on while digits are being dialed out (in both pulse and tone modes) and off at all other times.
20	20	$\overline{\text{MUTE}}$	Mute Output. N-channel open drain output. Output transistor is switched on during pulse dialing, off at all other times.
21	21	$\overline{\text{DP}}$	Dial pulse output. N-channel open drain output. The $\overline{\text{DP}}$ output falls to low (switched on) for break and flash operations during pulse dialing; it remains in a high impedance state (switched off) at all other times.

Operations

Symbol Definitions:

a. Dp: Pulse digit; 1, 2, 3, 4, 5, 6, 7, 8, 9, 0.
b. Dt: Tone digit; 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #.
c. Mj: Repertory memory; M1, M2, M3, . . . M20.
d. LOCi: i = 01, 02, . . . 09, 10, 11 . . . 20.
e. ZiZiZi: Conversation mode.
f. 0–0 ↑: Off-hook.
g. 0–0 ↓: On-hook.
h. ⌐↑ : Input level from low to high.
i. ↓¬ : Input level from high to low.
j. Dg: Digits for storing.
k. Mode select.

Recommended dialing, storing and clearing operations

a. Normal dialing in pulse mode
0–0 ↑, Dp . . . . . Dp; ZiZiZi . . . . . , 0–0 ↓
b. Normal dialing in tone mode
0–0 ↑, Dt . . . . . Dt; ZiZiZi . . . . . , 0–0 ↓
c. Mixed dialing (Pulse to tone mode)
1. 0–0 ↑, Dp . . . . . Dp, Mode select ↓¬ , Dt . . . Dt; ZiZiZi; 0–0 ↓ (Use mode select)
2. 0–0 ↑, Dp . . . . . Dp, T, Dt . . . Dt, ZiZiZi; 0–0 ↓ (Use T key)
d. Redialing
0–0 ↑, Dp . . . Dp, Mode Select ↓¬ , Dt . . . Dt; 0–0 ↓
0–0 ↑, [R/P], ZiZiZi. 0–0 ↓
e. Repertory dialing for one memory
1. 0–0 ↑, Mj, ZiZiZi, 0–0 ↓
2. 0–0 ↑, [A/L] LOCi, ZiZiZi, 0–0 ↓
f. Repertory dialing with cascaded memory (three memories or less)
1. 0–0 ↑, Mj1, Mj2, Mj3, ZiZiZi, 0–0 ↓
2. 0–0 ↑, [A/L] LOCi1, [A/L] LOCi2, [A/L] LOCi3, ZiZiZi, 0–0 ↓
g. Repertory dialing with cascaded memory (more than three memories)
1. 0–0 ↑, Mj1, Mj2, Mj3, (wait for all digits to dial out), Mj4, ZiZiZi, 0–0 ↓
2. 0–0 ↑, [A/L] LOCi1, [A/L] LOCi2, [A/L] LOCi3, (wait for all digit dial out), [A/L] LOCi4, ZiZiZi, 0–0 ↓
h. Store repertory memories using store-key (Off-hook store mode) (Note 2)
1. 0–0 ↑, [S], Dg . . . . . Dg, Mj, 0–0 ↓ (or [S]) (Direct store) (Note 2)
2. 0–0 ↑, [S], Dg . . . . . Dg, [A/L] LOCi, 0–0 ↓ (or [S]) (Indirect store)
i. Store repertory memories using store pin (Off-hook store mode)
1. 0–0 ↑, Store ⌐↑ , Dg . . . . . Dg, Mj1, Dg . . . Dg, Mj2 . . . Store ↓¬
2. 0–0 ↑, Store ⌐↑ , Dg . . . . . Dg, [A/L] LOCi1, Dg . . . Dg, [A/L] LOCi2, Store ↓¬

Note: 1. On-Hook/Off-Hook storage is controlled by the ON/$\overline{OFF}$ pin. On Hook storage uses the same process as described above, except that ON/$\overline{OFF}$ = V_{DD} and $\overline{HK}$ = V_{DD}.
2. The chip will remain in the Store mode unless the Store key is pressed again or the telephone handset is hung up.

j. The Flash key function
1. 0–0 ↑, [S], F, Dg . . . . . Dg, Mj or [A/L] LOCi, 0–0 ↓
0–0 ↑, Mj or [A/L] LOCi
O/P: F, Dg . . . . . Dg
2. 0–0 ↑, [S], Dg1, Dg2, Dg3, F, . . . Dgn, Mj or [A/L] LOCi, 0–0 ↓
0–0 ↑, Mj or [A/L] LOCi
O/P: Dg1, Dg2, Dg3, . . . Dgn (Flash code is ignored)
3. 0–0 ↑, Dg1, Dg2, F, Dg3 . . . Dgn, 0–0 ↓
0–0 ↑, R/P
O/P: Dg1, Dg2
k. Direct and indirect memory location cross reference

Direct Mode Memory Location	Indirect Mode Memory Location
M1	11
M2	12
M3	13
M4	18
M5	17
M6	16
M7	15
M8	14
M9	10
M10	19
M11	01
M12	02
M13	03
M14	08
M15	07
M16	06
M17	05
M18	04
M19	20
M20	09

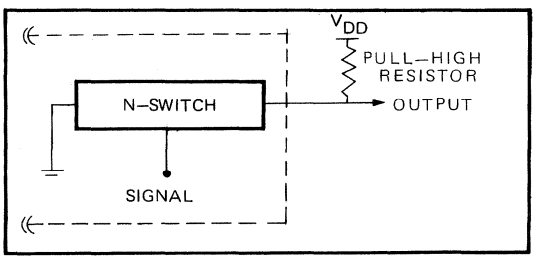
The memory locations of the UM91271 series do not correspond exactly for direct and indirect operations. That is, the telephone number stored in location M1, for example, is not equivalent to that of location 01 in indirect operation. The cross reference table above shows the corresponding memory locations for direct and indirect operations:

Examples:

1. Storing a telephone number into memory location 4
   a. Direct mode operation:
      0–0 ↑:[S],7152455,[M4],0–0 ↓.
   or b. Indirect mode operation:
      0–0 ↑:[S],7152455,[A/L],18, 0–0 ↓.
2. Recalling a telephone number from memory location 4
   a. Direct mode operation:
      0–0 ↑:[M4],ZiZiZi . . . 0–0 ↓.
   or b. Indirect mode operation:
      0–0 ↑:[A/L],18, ZiZiZi . . . 0–0 ↓.

Functional Description

a. N-Channel open drain output: $\overline{DP}$, $\overline{MUTE}$, $\overline{XMUTE}$, $\overline{MODE\ OUT}$.



b. DTMF Generator

This device has a well designed 6-level, 12-segment stable reference voltage and a fired output amplitude DTMF generator. The generator consists of a reference voltage regulator and a bipolar emitter follower that provides a V_{DD} – 1.8V reference voltage and approximately 1.2 volts of tone output swing.

The Total Harmonic Distortion (THD) of the UM91271 is a maximum of 5% at V_{DD} = 2 to 5V and frequency = 500 to 3400 Hz.

Level	Row	Column	Unit
C	V_{DDT} – 1.2	V_{DDT} – 1.2	V
1	V_{DDT} – 1.31	V_{DDT} – 1.108	V
2	V_{DDT} – 1.012	V_{DDT} – 0.949	V
3	V_{DDT} – 0.874	V_{DDT} – 0.765	V
4	V_{DDT} – 0.755	V_{DDT} – 0.606	V
5	V_{DDT} – 0.686	V_{DDT} – 0.514	V

Note: The listings above are typical values for reference only.

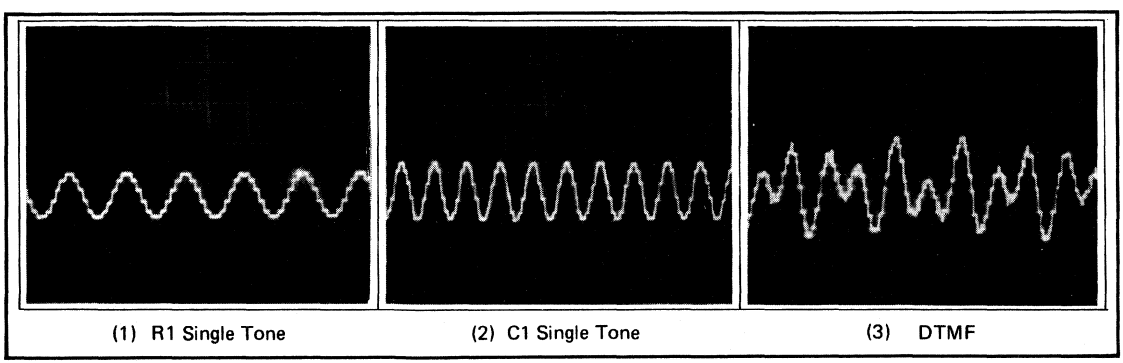
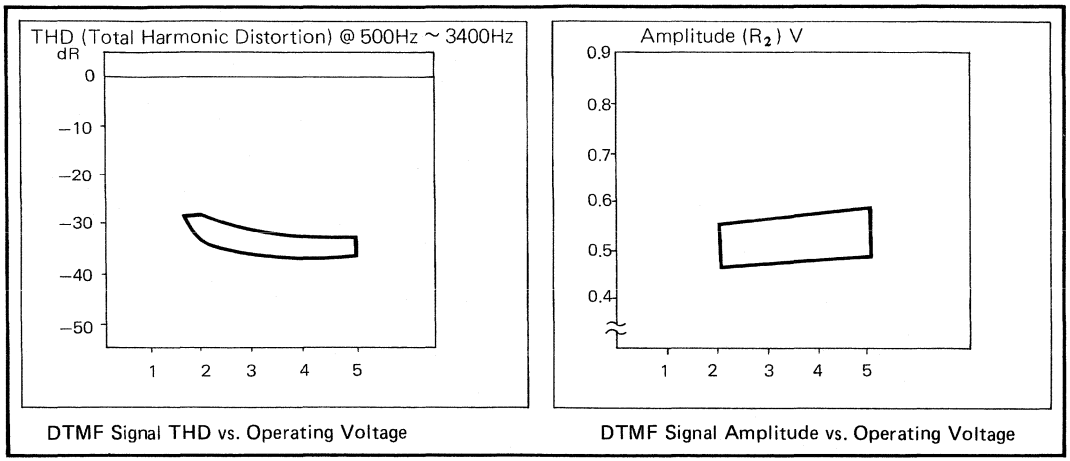


Figure 1 Waveforms



DTMF Signal THD vs. Operating Voltage

DTMF Signal Amplitude vs. Operating Voltage

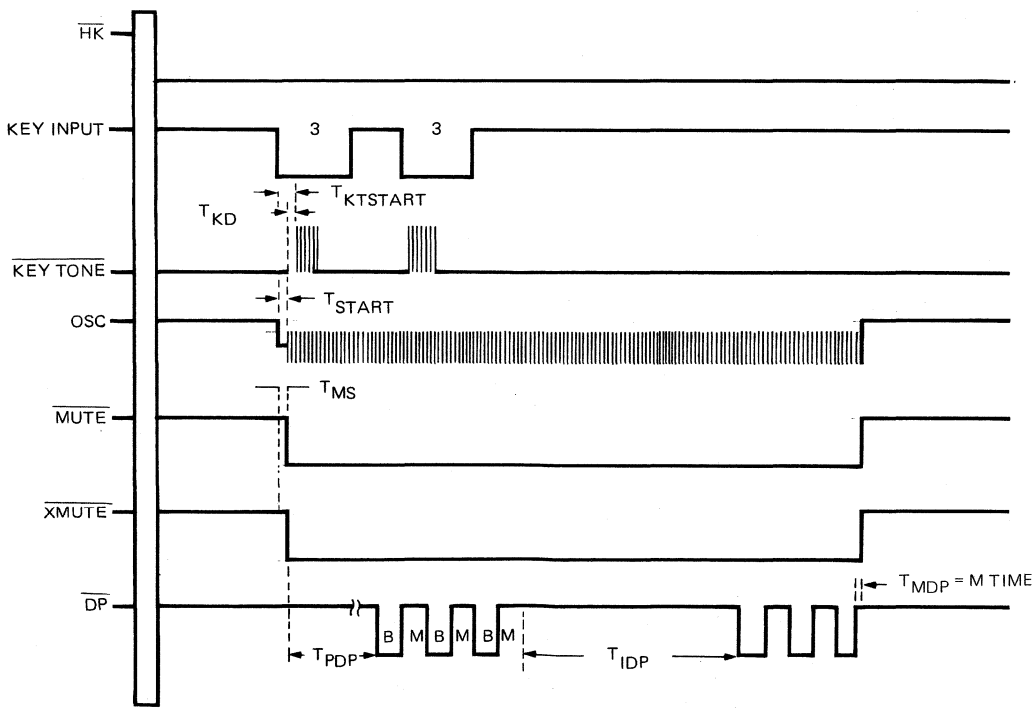
Figure 2

Figure 3

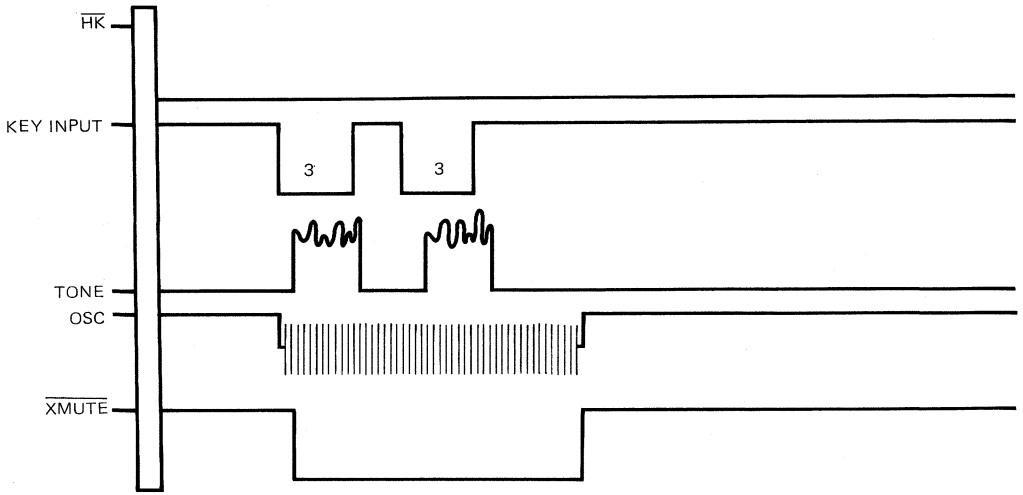
DTMF Signal THD vs. Operating Voltage and DTMF Output Amplitude vs. Operating Voltage are shown in figures 2 and 3 for reference in application design.

Timing Diagrams

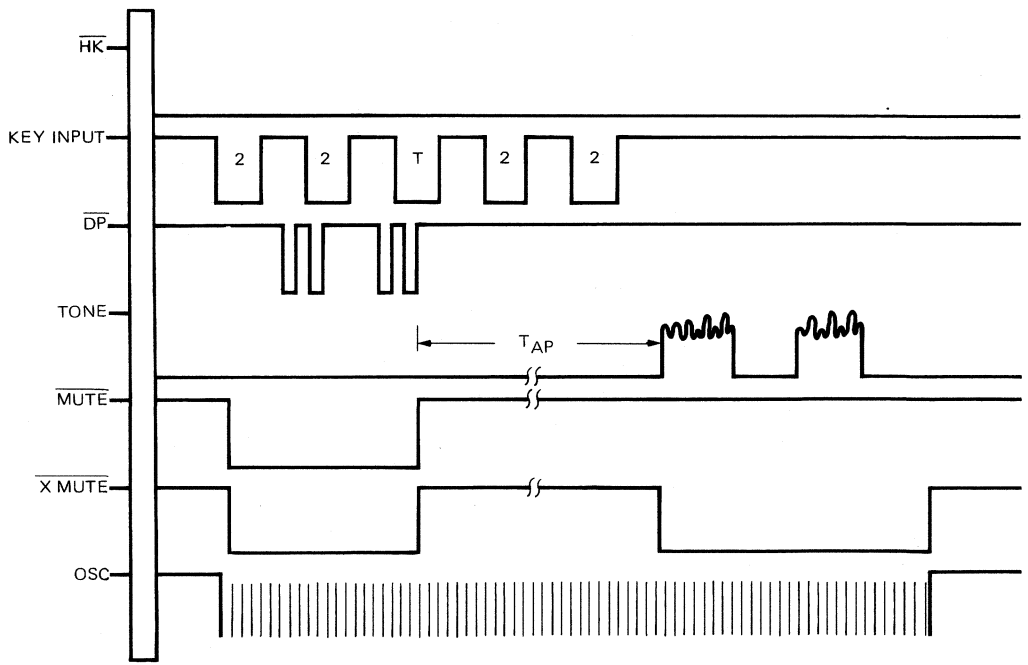
(1) PULSE MODE TIMING DIAGRAM



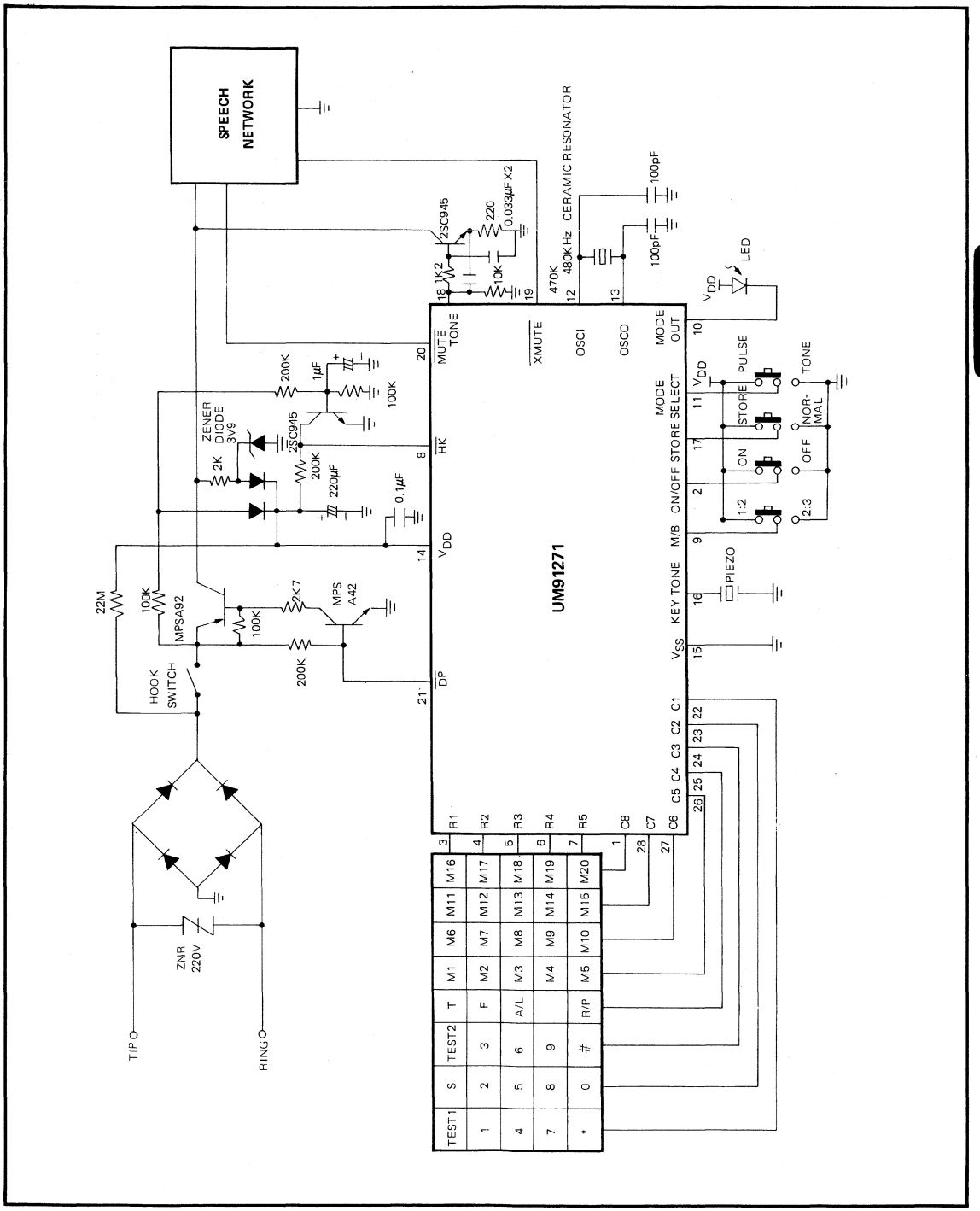
(2) TONE MODE TIMING DIAGRAM



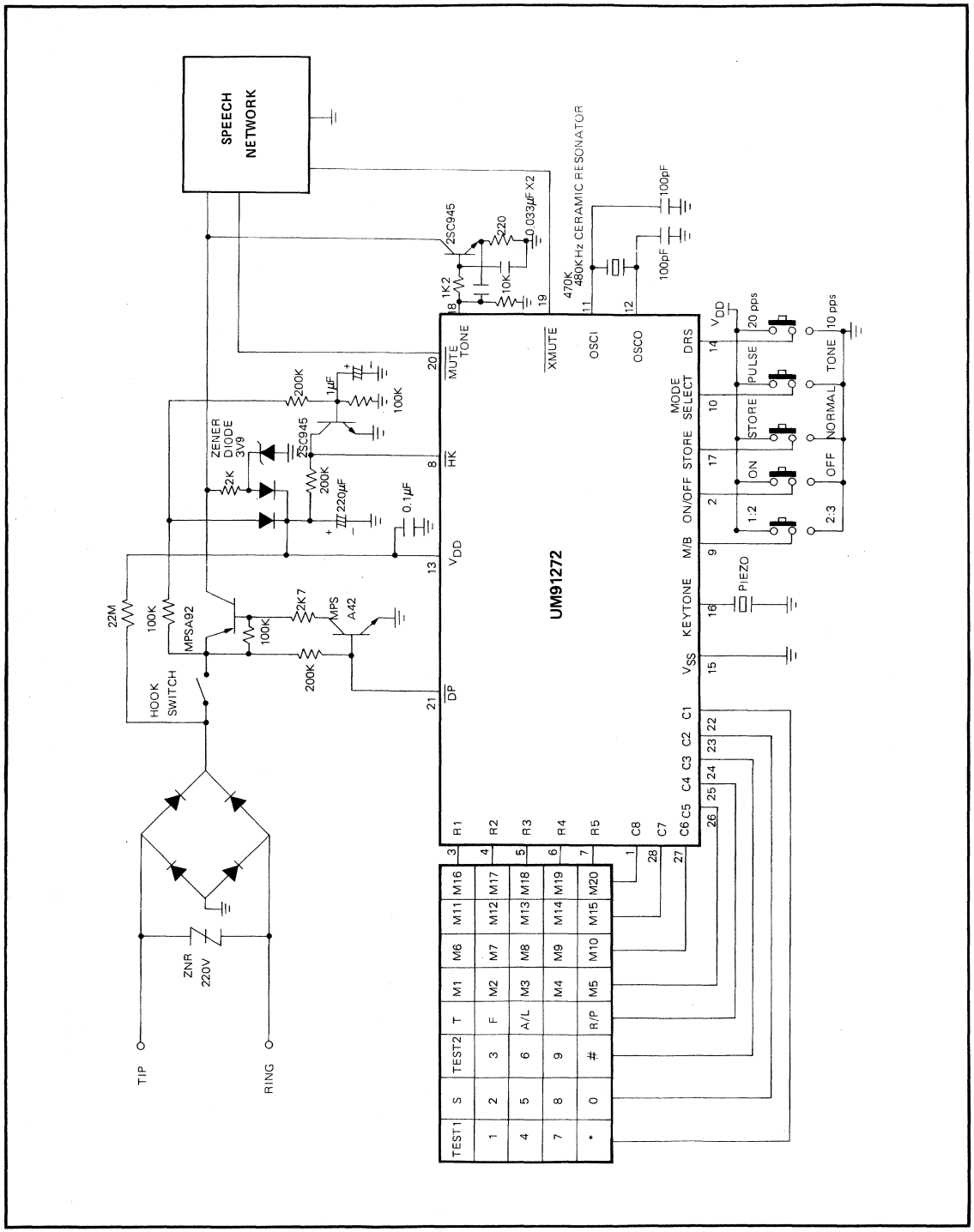
(3) NORMAL PULSE TO TONE MIXED DIALING VIA "T" KEY



Application Circuits

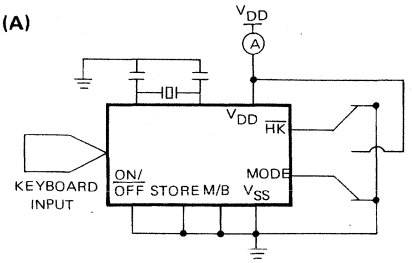


Application Circuits (Continued)

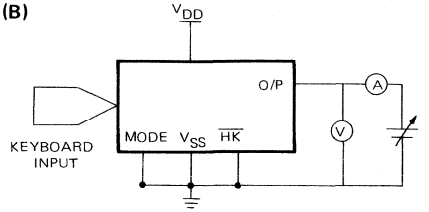


Test Circuits

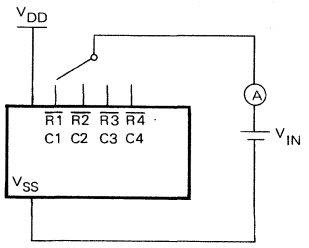
(A)



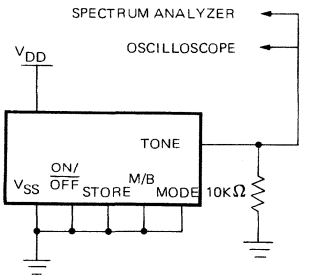
(B)



(C)



(D)



Tone/Pulse Dialer

UMC

UM91310 Series

TONE/PULSE DIALER

Features

- Pulse and DTMF dialing
- Memory clear function
- Four extra function keys: pause, flash, redial, and pulse to DTMF dialing (mixed mode)
- DTMF dialing:
  Manual dialing – minimum duration for bursts and pauses
  Redialing – calibrated timing
- On-chip oscillator uses low-cost 3.579545 MHz crystal
- Keyboard entry fully debounced
- 23 digits for redial operation
- Special function for flash operation
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion
- Uses standard 5 x 4 keyboard
- Flash (register recall) output

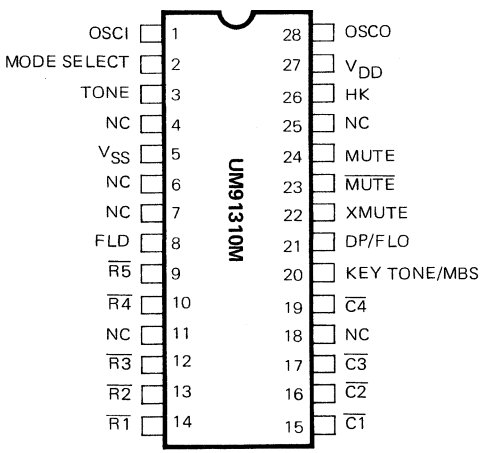
General Description

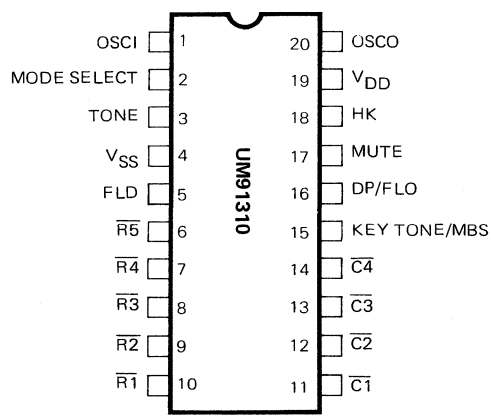
UM91310 is a single chip silicon gate CMOS integrated circuit with an on chip filter. It also provides an on chip oscillator for a 3.579545 MHz crystal.

Standard 5x4 matrix keyboard is used for either pulse dialing (PD) or dual tone multi-frequency (DTMF) mode. Up to 23 digits can be stored in on-chip RAM for redial.

In DTMF mode, minimum tone duration and minimum inter-tone pause are provided for fast key depressing. Maximum tone duration depends on the key depress time in manual dialing.

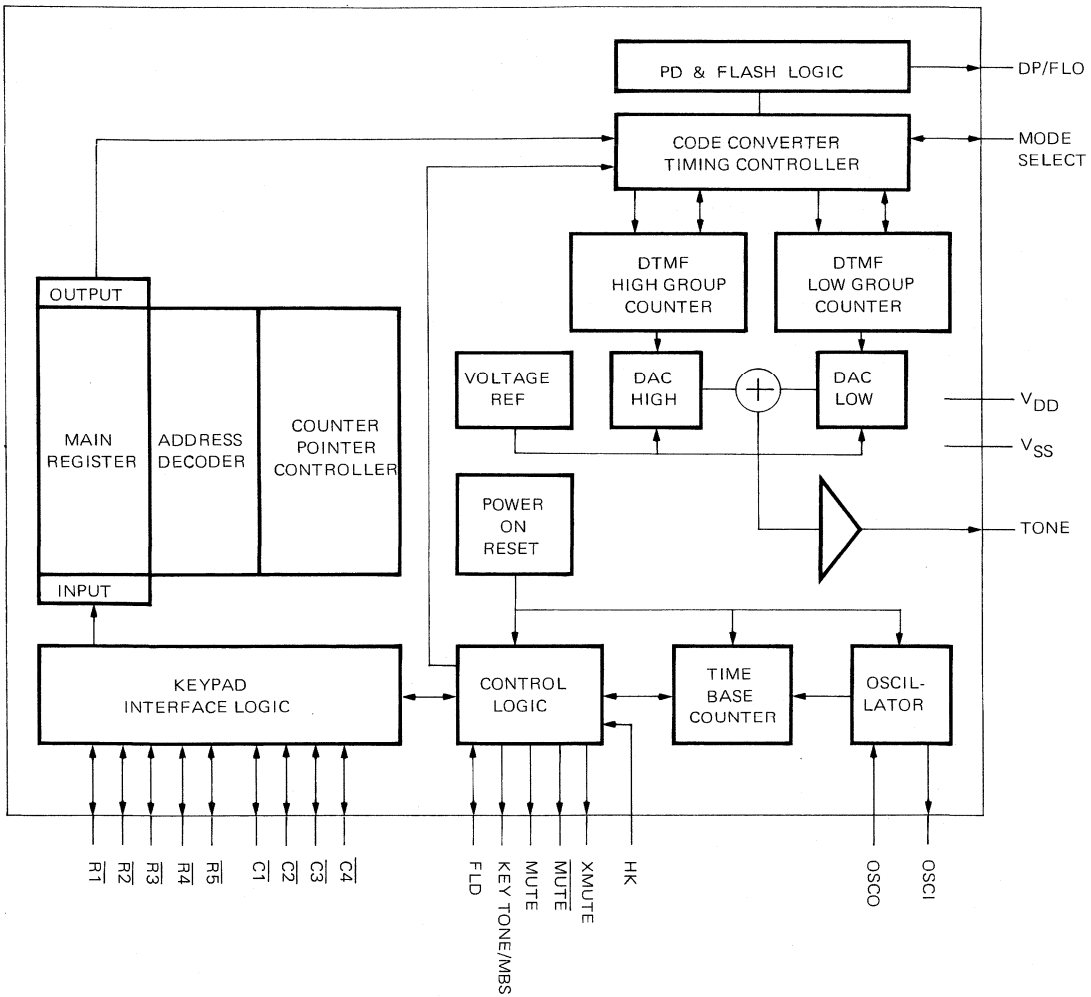
Pin Configurations





Note: The function of KEY TONE/MBS is determined by bond pad selection.

Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage V_{DD} (With respect to V_{SS})
. . . . . –0.8 to 6V
Supply Current I_{DD} . . . . . 50 mA
All Input Voltages . . . . . –0.8V to V_{DD} + 0.8V
DC Current Into Any Input or Output . . . . . 10 mA
Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . –60 to 150°C
Total Power Dissipation . . . . . 300 mW
Power Dissipation Per Output . . . . . 50 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = 3V, V_{SS} = 0V, Crystal: 3.579545 MHz; R_S = 100 Ω max.; T_A = 25°C; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage						
Operating supply voltage	V_{DD}	2.5	–	5.0	V	
Memory retention voltage	V_{MR}	1.8	–	5.0	V	
Operating Supply Current						
Conversation mode	I_{DDC}	–	–	150	μA	Osc. ON
Pulse dialing or Flash	I_{DDP}	–	–	400	μA	
DTMF dialing	I_{DDT1}	–	0.6	1.2	mA	Tone ON
DTMF dialing	I_{DDT2}	–	–	200	μA	Tone OFF
Standby Supply Current	I_{SD}	–	–	5	μA	V_{DD} = 1.8V; T_{AMB} = 25°C Osc. OFF (Note 1)
Inputs						
Input voltage Low of any pin	V_{IL}	0	–	0.3 V_{DD}	V	
Input Voltage HIGH of any pin	V_{IH}	0.7 V_{DD}	–	V_{DD}	V	
Input leakage current of HK	I_{IL}	–	–	± 1	μA	
Keyboard on Current	I_{ON}	–	–	45	μA	
Outputs						
Output sink current for MUTE, $\overline{\text{MUTE}}$, XMUTE, DP/FLO, KEY TONE, FLD	I_{OL1}	0.7	–	–	mA	at V_{OL} = V_{SS} + 0.5V
MODE SELECT (note 2)	I_{OL2}	–	1	–	mA	
Output source current for MUTE, $\overline{\text{MUTE}}$, XMUTE, DP/FLO, KEY TONE, FLD	I_{OH1}	0.6	–	–	mA	at V_{OH} @ V_{DD} – 0.5V
MODE SELECT (note 2)	I_{OH2}	–	10	–	μA	
FLD (note 3)	I_{OH3}	–	100	–	nA	

DC Electrical Characteristics (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TONE OUTPUT						
DTMF output voltage levels (r. m. s.) for						at V_{DD} = 2.5 to 5V
HIGH group	V_{OC} (rms)	158	192	205	mV	
LOW group	V_{OR} (rms)	125	150	160	mV	
D. C. voltage level	V_{DD}	–	½ V_{DD}	–	V	
Output impedance	|Zo|	–	–	1.5	KΩ	
Pre-emphasis of group	T_{WIST}	1.85	2.1	2.35	db	
Total harmonic distortion (note 4)	T_{HD}	–	–20	–	db	

AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Tone Output						
Frequency deviation	df/f	–0.6	–	0.6	%	at V_{DD} = 2.5 to 5V
Timing and Frequency						
Oscillator start-up time	T_P	–	10	–	ms	
Key pad debounce time	T_{KD}	–	15	–	ms	
Reset delay time	T_{RD}	–	160	–	ms	
Transmission and pause Time						
Tone duration for	T_{MFD} T_{TIDP}					
Manual dialing		68	–	–	ms	
Redialing		68	70	72	ms	
Flash pulse duration	T_{FL}	98	100	102	ms	
Flash hold-over time	T_{FLH}	29	30	31	ms	
Hold-over time (muting on MUTE)	T_H	78	80	81	ms	
Pulse Dialing (PD)						
Dial pulse rate	DR	9.8	10	10.4	Hz	
Inter-digit pause	T_{IDP}	828	840	844	ms	
Break time MBS = V_{DD}	TB1	65	67	68	ms	
MBS = V_{SS}	TB2	59	60	61	ms	
Make time MBS = V_{DD}	TM1	31	33	34	ms	
MBS = V_{SS}	TM2	39	40	41	ms	

Notes to the DC and AC Electrical characteristics

1. Crystal connected between OSCI and OSCO; HK at V_{SS} and all other pins open-circuited.
2. |10 mA| dynamic current to set/reset MODE SELECT pin (mixed mode)
3. Flash inactive; V_{OH} = V_{SS}.
4. Related to the level of the LOW group frequency component (PTT ELR 305).

Pin Description

28 (20) Pin No.	Symbol	I/O	Description
1 (1) 28 (20)	OSCI OSCO	I O	Oscillator input and output pins: The time base for UM91310 is a crystal controlled on-chip oscillator which is completed by connecting a 3.579545 MHz crystal between the OSCI and OSCO pins.
2 (2)	MODE SELECT	I	Mode selection: There are three operating modes in UM91310 – PD mode, DTMF mode, and mixed mode. This pin selects which mode the UM91310 will operate on. PD mode If MODE SELECT = V_{SS}, then pulse mode is selected. Entries of non-numeric keys are neglected, and neither stored in the redial register nor transmitted. DTMF mode If MODE SELECT = V_{DD}, then DTMF mode is selected. Each non-function pushbutton activated corresponds to a combination of two tones, each one of four possible low and high group frequencies. These frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic constant. The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (TMFD) and or minimum pause time (TTIDP). Mixed mode When the MODE SELECT is open-circuited, then mixed mode is selected. After activation of HK or FL, the circuit starts as a pulse dialer and remains in this state until a non-numeric (A, B, C, D, *, #) or the ">" key is activated. Then the circuit changes to DTMF dialing and remains there until FL is activated or after a static standby condition, HK is re-activated. A touch between MODE SELECT pin and V_{DD} also initiates DTMF dialing. Hook switch HK, flash FL or a connection of MODE SELECT pin to V_{SS} sets the circuit back to pulse dialing.
3 (3)	TONE	O	Tone output: The single and dual tones which are provided at the TONE output are filtered by an on chip filter. The total harmonic distortion of the DTMF tone falls within PTT ELR 305 recommendations. An on-chip reference voltage provides output tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signaling. When the DTMF mode is selected output tones are timed in manual dialing with a minimum duration of bursts and pauses, and in redial with calibrated timing. Single tones may be generated for test purposes (HK = high). Each row and column has one corresponding frequency. By connecting the column/row to V_{SS}, the corresponding high/low single tone frequency is generated. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Pin Description (Continued)

28 (20) Pin No.	Symbol	I/O	Description
27 (19)	V_{DD}	P	Positive and negative power supply: The positive power supply for the circuit must meet the voltage requirements indicated in the electrical characteristics table. To avoid undefined states of the device when powered on, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum memory retention supply voltage of 1.8 volts, the memory may be destroyed. The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay, regardless of the state of Hook switch HK.
5 (4)	V_{SS}	P	
8 (5)	FLD	I/O	Flash duration control: Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialing modes. Pressing the FL key will produce a timed line break of 100 ms (min.) at the DP/FLO output. While in the conversation mode, the flash pulse entry will act as a chip enable. The flash pulse duration (TFL) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig. 2). The FL key has special functions in the redial mode (see redial procedure with the flash inserted telephone number).
9 (6)	$\overline{R5}$	I/O	Keyboard inputs/outputs: The keyboard layout of UM91310 is shown in Fig. 3. All keyboard entries are debounced for an approximate time of TKD. Each entry is tested for validity. When a pushbutton is pressed, keyboard scanning begins and the chip returns to the sense mode only after the pushbutton is released. Rt of the keyboard contains the following special function keys: * P Auto pause * FL Flash or register recall * R Redial * > Changes of dial mode from PD to DTMF in mixed dialing In pulse dialing mode, the valid keys are the 10 numeric keys (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on dialing or redial storage. The valid function keys are P, FL, and R. In the DTMF mode, all nonfunction keys are valid. They are transmitted as dual-tone combinations and, at the same time are stored in the redial register. P, FL, and R are valid function keys. In mixed mode dialing, all key entries are valid and are executed accordingly. The P key executes a pause for 2.5 to 3 seconds. If the key is pressed again during the pause period, it will release the pause function.
10 (7)	$\overline{R4}$	I/O	
12 (8)	$\overline{R3}$	I/O	
13 (9)	$\overline{R2}$	I/O	
14 (10)	$\overline{R1}$	I/O	
19 (14)	$\overline{C4}$	I/O	
17 (13)	$\overline{C3}$	I/O	
16 (12)	$\overline{C2}$	I/O	
15 (11)	$\overline{C1}$	I/O	

Pin Description (Continued)

28 (20) Pin No.	Symbol	I/O	Description
20 (15)	KEY TONE MBS	O or I	Key in tone output or Make break ratio selection: The function of this pin is selected by bonding option. A 1.19 KHz key-in tone output is provided to produce audible feedback for key entries. UM91310B and UM91310BM do not provide this key-in tone output. This input pin is used to select the pulse dialing make/break ratio. When MBS is equal to V_{DD}, the make/break ratio is 1:2. When MBS = V_{SS}, the make/break ratio is 2:3. The 28-pin package is provided with these bonding options.
21 (16)	DP/FLO	O	Dial pulse and flash output: This is a combined output which provides control signals for proper timing in pulse dialing or for a calibrated break in both dialing modes (flash or register recall).
22	XMUTE	O	Strobe output: This output remains active high during actual dialing: i. e., during break or make time in pulse dialing, or during tone on in DTMF dialing.
23 24 (17)	$\overline{\text{MUTE}}$ MUTE	O O	$\overline{\text{MUTE}}$ and MUTE output: In pulse dialing mode, the mute output becomes active high for the period of the inter-digit pause, break time and make time. In tone dialing mode, the mute output becomes active high during DTMF on and hold-over time. It remains at this level until the last digit has been output. $\overline{\text{MUTE}}$ the inverted output of MUTE.
26 (18)	HK	I	Hook switch: The HK input enables the circuit and is used to initialize the IC. HK is Low during the static standby condition. In this state, the clock oscillator is disabled and all registers and logic are reset, with the exception of Write Address Counter (WAC). The Write Address Counter (WAC) points to the last entered digit. The keyboard input is inhibited, but the data previously entered is saved to the redial register as long as V_{DD} is higher than VMR (min.) The current drawn is ISD (standby current) and serves to retain data in the redial register while the phone is in an on-hook condition. If HK is high, the clock oscillator is activated and the circuit changes from a static standby condition to the conversation mode. The current is IDDC until the first digit is entered from the keyboard. Then, a dialing or redialing operation is initiated. The operating current is IDDP if in the pulse dialing mode or IDDF in the DTMF dialing mode. If the HK input is taken low for more than time TRD (see Fig. 5a Fig. 5b and timing data), an internal reset pulse will be generated at the end of the TRD period. The system changes to the static standby state. A short HK pulse of less than TRD will not affect the operation of the circuit and reset pulses are not produced.

Table 1. Frequency tolerance of the output tones for DTMF signaling.

Row/ Column	Standard Frequency (Hz)	Tone Output Frequency (Hz)	Frequency Deviation	
			Hz	%
Row 1	697	696.95	–0.05	–0.01
Row 2	770	768.80	–1.20	–0.16
Row 3	852	852.27	+0.27	–0.03
Row 4	941	943.97	+2.97	+0.32
Col 1	1209	1212.58	+3.58	+0.30
Col 2	1336	1331.68	–4.32	–0.32
Col 3	1477	1476.71	–0.29	–0.02
Col 4	1633	1638.99	+5.99	+0.37

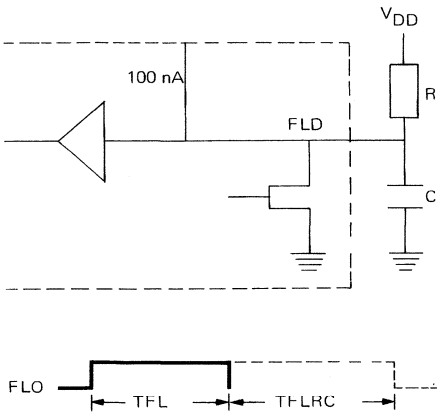
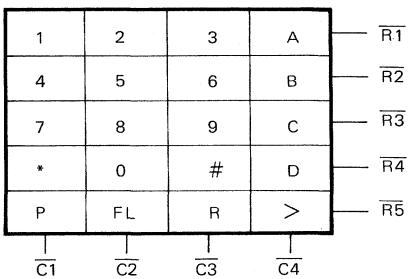


Fig. 2. Flash pulse duration setting



P: Pause
FL: Flash
R: Redial
>: Changes dial mode from PD to DTMF in Mixed

Fig. 3. Keyboard layout

Functional Description

Part 1. Operation procedures

Dialing

After HK has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 4). When the first valid digit is entered, the Temporary Write Address Counter (TWAC) is set to the first address, the decoded digit is stored in the register, and the TWAC is incremented to the next address. Any subsequent keyboard entry is then decoded and stored in the redial register after validation. The first five valid entries have no effect on the main register and its associated write address counter.

After the sixth valid digit is entered, TWAC indicates an overflow condition. The data from the temporary register will be copied to the five least significant places of the main register and TWAC to the WAC. All the following digits (including the sixth digit) are stored in the main register (up to a total of 23). If more than 23 digits are entered, redial will be inhibited. If five digits or less are entered, only the temporary register and the associated TWAC are affected. All entries are debounced for at least the amount of time shown in Fig. 5. Each entry is tested for validity before being deposited in the redial register.

* In DTMF mode, all non-function keys are valid.
* In PD mode, only numeric keys are valid.

At the same time that they re accepted and depending on the mode selected (PD, DTMF or mixed), the entries are transmitted as PD pulse trains or as DTMF frequencies

in accordance with postal requirements. Entries other than numeric are ignored during pulse dialing. They are neither stored nor transmitted.

Redialing

After HK has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address. The UM91310 is in the conversation mode.

If "R" is the first keyboard entry the circuit starts transmitting the contents of the temporary register. If the overflow flag on the TWAC was set to the number previously dialed, dialing continues from the main register. If the flag was not set, the number residing in the temporary register will only be redialed until the temporary read and write registers are equal.

Before the "R" is pressed, a dialing sequence of up to five digits is possible. If these digits are equal to the corresponding digits in the main register, redial continues with the main register until the last digit stored is transmitted.

In the DTMF mode, timing is calibrated for both tone bursts and pauses.

In mixed mode, only the first part entered (the pulses that were dialed as part of the stored number) can be redialed.

When redial is active, keyboard entries (both function and numeric) will not be accepted until the circuit returns to the conversation mode after redial is complete.

No redial activity can be performed when any of the following events take place:

* The power-on test.
* Memory clear ("R" or "FL" without additional data entry).
* Memory overflow (more than 23 valid data entries).

Part 2. Keyboard and switches operation

1. Symbol Definition:

a. Dp : PULSE dialing digit data: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, P.

b. Dt : TONE dialing digit data: *, #, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, A, B, C, D, P.

c. → : PULSE to DTMF key in mixed mode: >, *, #, A, B, C, D.

d. zizizi : Conversation mode.

e. 0–0 ↑ : Off-Hook.

f. 0–0 ↓ : On-Hook.

g. ⌐ : Input level from low to high.

h. ¬ : Input level from high to low.

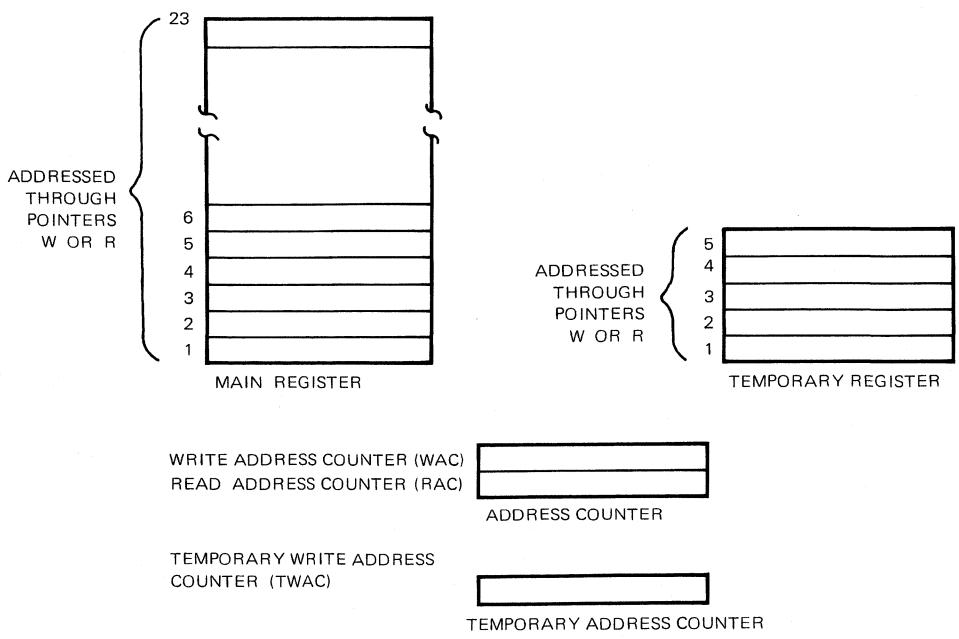


Fig. 4 Program Memory Map

i. $\neq$: not equal.

j. $>$: greater than.

k. $\leqslant$: less than or equal to.

l. Dg : Dialing digit (pulse or tone).

2. Recommended Dialing, Redialing and Clear Operations:

a. Normal dialing and redialing in pulse mode (MODE SELECT = V_{SS})

0–0 ↑; Dp, . . . , Dp; zizizi; 0–0 ↓

0–0 ↑; R; Dp, . . . , Dp out; zizizi; 0–0 ↓

b. Normal dialing and redialing in tone mode (MODE SELECT = V_{DD}).

0–0 ↑; Dt, . . . , Dt; zizizi; 0–0 ↓

0–0 ↑; R; Dt, . . . , Dt out; zizizi; 0–0 ↓

c. Mixed dialing via MODE SELECT pin.

0–0 ↑; Dp, . . . , Dp; MODE SELECT ⌐¯

Dt, . . , Dt; zizizi; 0–0 ↓

d. Mixed dialing and redialing via keypad (MODE SELECT open)

0–0 ↑; Dp, . . . , Dp, →; Dt, . . . , Dt; zizizi; 0–0 ↓

0–0 ↑; R; Dp . . . , Dp; zizizi; 0–0 ↓

(Note: If the digits dialed in the above dialing operations exceed 23, redialing operation will be inhibited.)

e. Redial operations about Main register and Temporary register: power on

0–0 ↑; Dga1, . . . , Dgai 0–0 ↓

0–0 ↑; Dgb1, . . . , Dgbj 0–0 ↓

(i, j $\leqslant$ 23)

(1) ai $\leqslant$ 5, bj $\leqslant$ 5

0–0 ↑; R; Dgb1, . . . , Dgbj out; or

0–0 ↑; Dgc1, . . . , Dgck; R; no digit out after R key.

(2) ai $\leqslant$ 5, bj $>$ 5

0–0 ↑; R; Dgb1, . . . , Dgbj out; or

0–0 ↑; Dgc1, . . . , Dgck; R;

If ck $\leqslant$ 5 and Dgct = Dgbt (t = 1 . . k) then Dgbk+1, . . . , Dgbj out

If ck $>$ 5 or Dgct $\neq$ Dgbt (t = 1 . . k $\leqslant$ 5) then no digit out after R key

(3) ai $>$ 5, bj $\leqslant$ 5

0–0 ↑; R; Dgb1, . . . , Dgbj out; or

0–0 ↑; Dgc1, . . , Dgck; R;

If ck $\leqslant$ 5 and Dgct = Dgat (t = 1 . . k) then Dgat+1, . . . , Dgai out

if ck $>$ 5 or Dgct $\neq$ Dgat (t = 1. . k $\leqslant$ 5) then no digit out after R key

(4) ai $>$ 5, bj $>$ 5

0–0 ↑; R; Dgb1, . . . , Dgbj out; or

0–0 ↑; Dgc1, . . . , Dgck; R;

if ck $\leqslant$ 5 and Dgct = Dgbt (t = 1. . k) then Dgbk+1 . . . , Dgbj out

if ck $>$ 5 or Dgct $\neq$ Dgbt (t = 1. . k $\leqslant$ 5) then no digit out after R key

f. Special operation on * and #:

(1) 0–0 ↑; Dg1, . . . , Dgi; * or #; Dgi+1, . . . , Dgn; zizizi; 0–0

0–0 ↑; R; Dg1, . . . , Dgi out 0–0 ↓

(2) 0–0 ↑; * or #; Dg1, . . . , Dgi; zizizi; 0–0 ↓

0–0 ↑; R; * or #; Dg1, . . . , Dgi out; 0–0 ↓

g. Special Operation on FL key:

0–0 ↑; Dg, . . . , Dgi; FL; Dgi+1, . . . , Dgn; zizizi; 0–0 ↓

0–0 ↑; R; Dgi + 1 . . . , Dgn out; 0–0 ↓

h. Clearing redial buffer by using R key

0–0 ↑; Dg1, . . , Dgi (i $>$ 5); R; 0–0 ↓

0–0 ↑; R; no digit out

Timing Diagrams

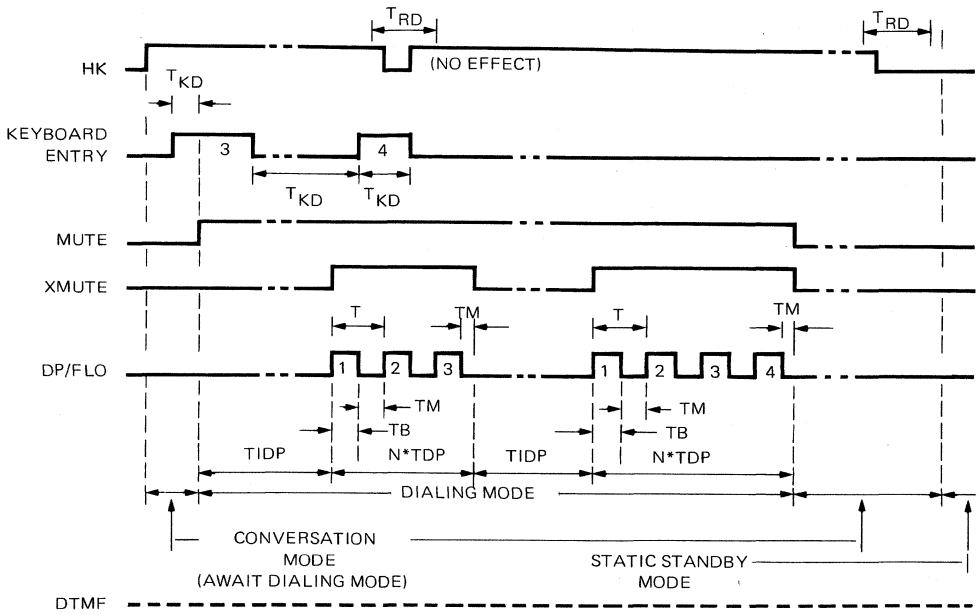


Fig. 5a Timing diagram for pulse mode (MODE SELECT = V_{SS})

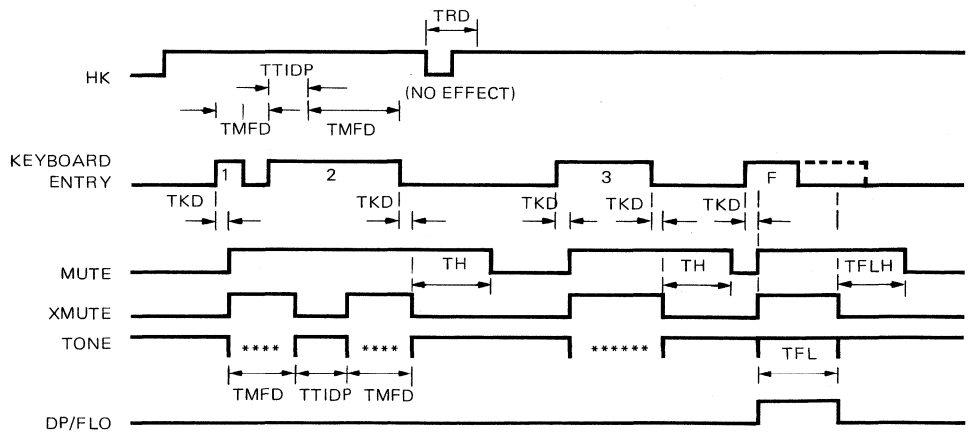


Fig. 5b Timing diagram for DTMF dialing mode (MODE SELECT = V_{DD})

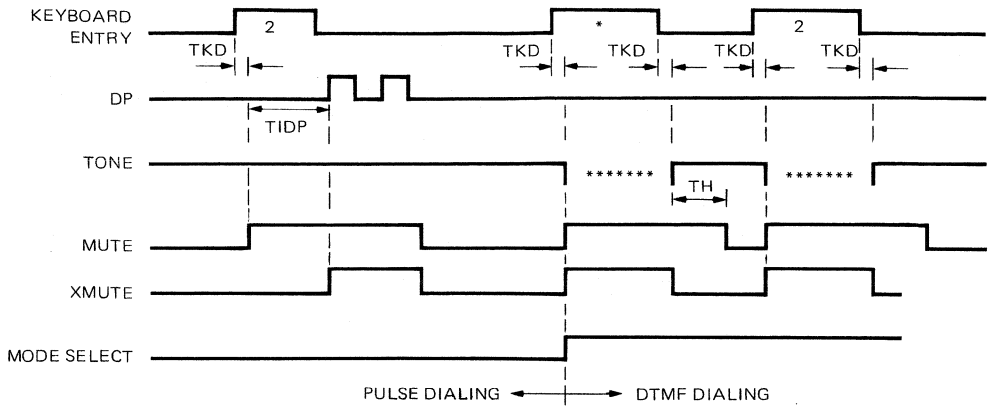


Fig. 5c Timing diagram for mixed dialing mode (MODE SELECT = open-circuit)

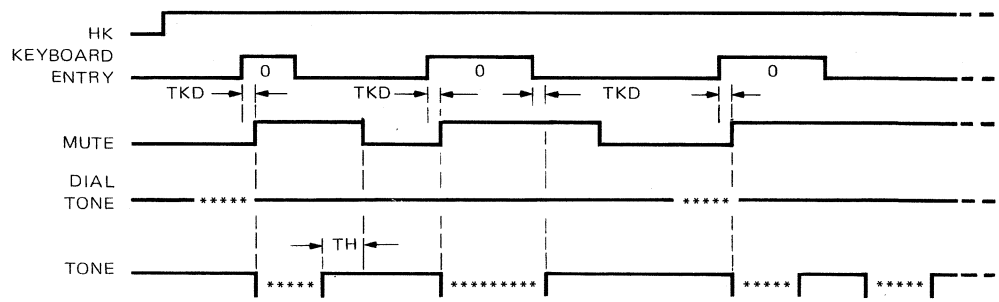
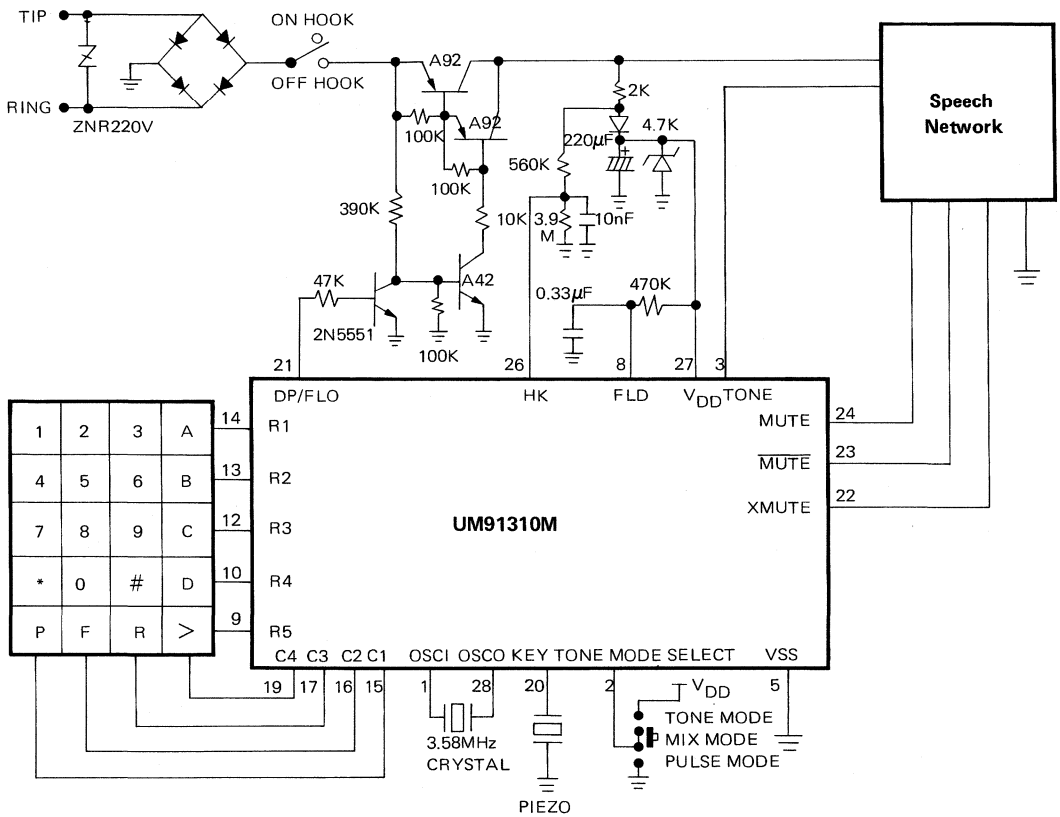


Fig. 5d Timing diagram showing REDIAL where PABX access digits are the first keyboard entries; DTMF dialing with MODE SELECT = V_{DD}

Application Circuit



Ordering Information

Part No.	M/B Ratio	Key-In Tone	Package
UM91310	1:2	Available	20 DIP
UM91310A	2:3	Available	20 DIP
UM91310B	Pin Selectable	Not Available	20 DIP
UM91310M	1:2	Available	28 SO
UM91310AM	2:3	Available	28 SO
UM91310BM	Pin Selectable	Not Available	28 SO

Tone Dialer

Part No.	Description	Page
UM95080/81	One-Key Dialer	3-3
UM95087	Tone Dialer	3-10
UM95088	Tone Dialer	3-17
UM95089	Tone Dialer	3-24
UM9559E/F	Tone Dialer	3-32

UMC

UM95080/81

One-Key Dialer

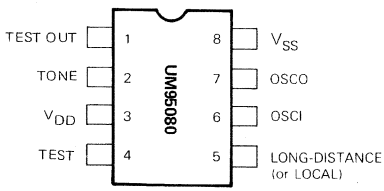
Features

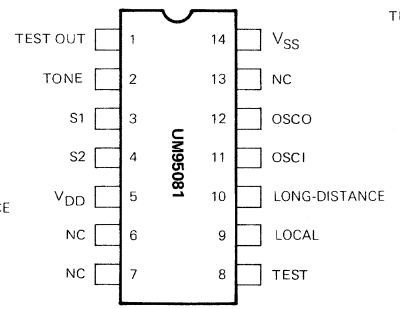
- Four 16-digit number memories
- Local/long distance call selection
- Wide operating voltage range: 2.0 to 5.0V
- Low standby current: 2μA typically (at V_{DD} = 3.0V)
- Uses 480KHz ceramic resonator
- Mask programming of customer-designated telephone numbers
- UM95080 is packaged in 8-pin DIP and provides dialing of one telephone number
- UM95081 is packaged in 14-pin DIP and UM95081M is in 20-pin SO, provide dialing of eight telephone numbers

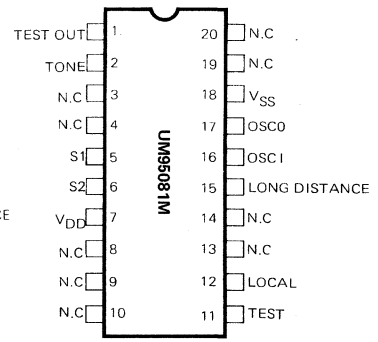
General Description

The UM95080/81 monolithic one-key dialers provide quick, convenient, one-key DTMF auto-dialing. The UM95080 is packaged in an 8-pin DIP and provides dialing of one telephone number through the use of a single trigger button. The UM95081 provides dialing of up to eight numbers through the use of two switches and local and long-distance dialing buttons.

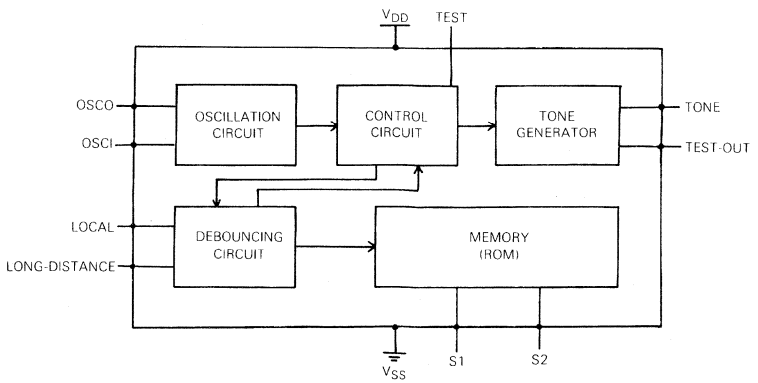
Pin Configurations







Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage..... −0.3V to 5.5V
Input Voltage..... −0.3V to V_{DD}+0.3V
Maximum Power Dissipation.....500 mW
Operating Temperature..... −20°C to +70°C
Storage Temperature..... −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD}=3.0V, F_{OSC}=480KHz, T_{OP}=25°C, unless otherwise specified)

Parameter	Symbol.	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD}	2.0		5.0	V		A
Standby Current	I_{SD}		2	5	μA	All outputs unloaded	B
Supply Operating Current	I_{DD}		0.7	1.5	mA	Oscillator running, all outputs unloaded	A
Input Voltage Range	V_{IH} V_{IL}	0.8 0		1 0.2	V_{DD}		A
Single Row Tone Output Amplitude	V_{OR}	620	670	720	mV	R_{LOAD} = 15KΩ	C
Single Column Tone Output Amplitude	V_{OC}	800	870	940	mV	R_{LOAD} = 15KΩ	C
Pre-emphasis	Twist	1	2	3			C
Valley of Single Tone	V_V		0.4		V_{DD}	R_{LOAD} = 15K	C
Distortion	DIS %			5	%		C

Note: $\text{DIS (\%)} = \dfrac{100(V1^2 + V2^2 + \ldots + Vn^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$

where

1. V1...Vn are the intermodulation and harmonic frequencies in the 500 to 3400 Hz band, and
2. V_{IL}, V_{IH} are the individual frequency components of the DTMF signal.

AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Keypad Debounce Time	T_{KD}		38			ms
Oscillator Start-up Time	T_{START}		8			ms
Minimum Tone Duration	T_{MFD}			99		ms
Min. Tone Inter-digital Pause	T_{TIDP}			108		ms

AC Characteristics (Continued)

Digit	Test Out Frequency	
	Row(Hz)	Column(Hz)
1	4182	7254
2	4182	8016
3	4182	8862
4	4620	7254
5	4620	8016
6	4620	8862
7	5112	7254
8	5112	8016
9	5112	8862
0	5646	8016

R/C	Condition	Spec.	Actual	Error(%)	Unit
R1	F_{OSC} = 480 KHz	697	695.65	−0.19	Hz
R2		770	769.23	−0.1	
R3		852	851.06	−0.11	
R4		941	941.18	+0.02	
C1		1209	1212.12	+0.26	
C2		1336	1333.33	−0.2	
C3		1477	1481.48	+0.3	

Pin Description

Pin		Designation	Description
95080	95081		
1	1	TEST OUT	Test output. This pin intermittently outputs low and high square waves of frequencies six times those of the selected tone.
2	2	TONE	Tone output (see functions)
	3, 4	S1, S2	Telephone number selection inputs. These pins select the telephone number to be dialed (UM95081 only).
3, 8	5, 14	V_{DD}, V_{SS}	Positive power supply. Negative power supply. Operating voltage range: 2.0V to 5.0V.
4	8	TEST	Test mode select input. This pin is held at active low internally. When this input is pulled high, the entire circuit shifts into test mode.
	9	LOCAL	Local call mode select input. Pulling this input high activates the local call dialing mode.
5	10	LONG-DISTANCE	Long-Distance call mode select input. Pulling this input high activates the long-distance call dialing mode.
6, 7	11, 12	OSCI, OSCO	Oscillator circuit Input/Output. A 480 KHz ceramic resonator and two 100pF serial loading capacitors form a complete oscillator circuit. The circuit is activated when $\overline{HS}$ is low. Oscillator start-up time is typically 10ms.

DTMF Generator

The UM95080/81 has a well-designed 6-level, 12-segment, 1/2 V_{DD} reference voltage. The DTMF output of the UM95080/81 typically has a THD (total harmonic distortion) of 5%, a very low value compared to the EIA RS-470 standard of 10%.

The temperature coefficients of the DTMF output amplitudes are balanced to zero by the adaptive DTMF generator Structure.

The output strength of the column tones is pre-emphasized 2.5 dB more than the row tones. The typical equivalent output impedance of the DTMF generator is 1.5 KΩ.

DTMF signal distortion vs. operating voltage and DTMF output amplitude vs. operating voltage is shown in figures 1 and 2 below.

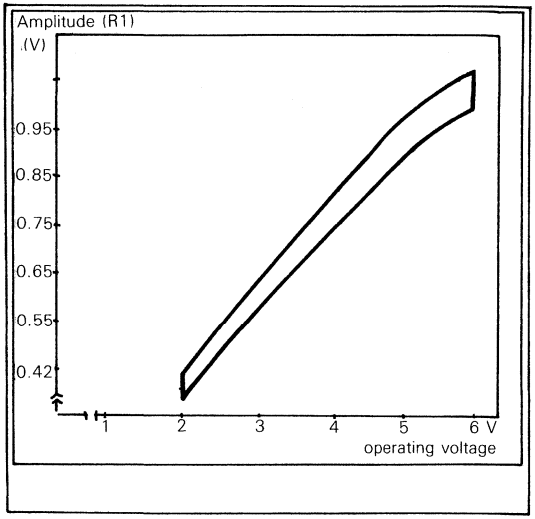


Figure 1.

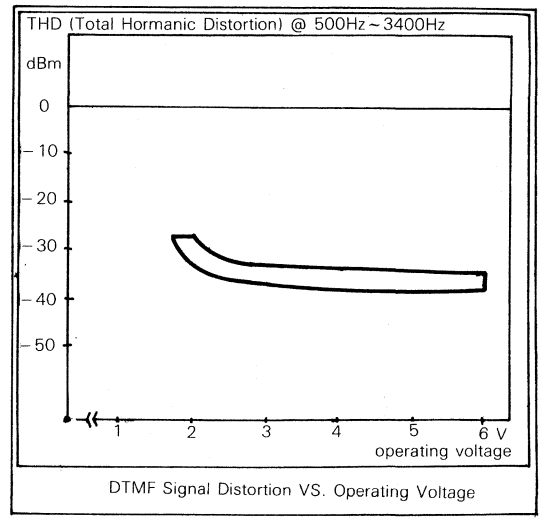


Figure 2.

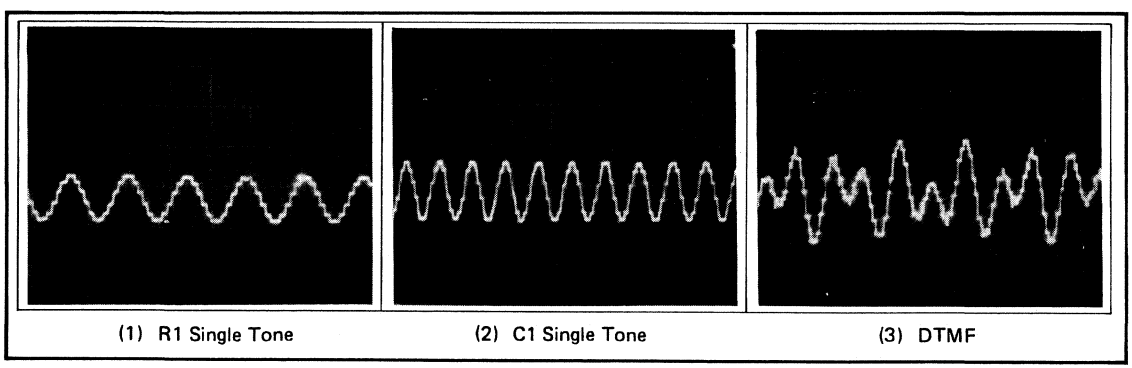
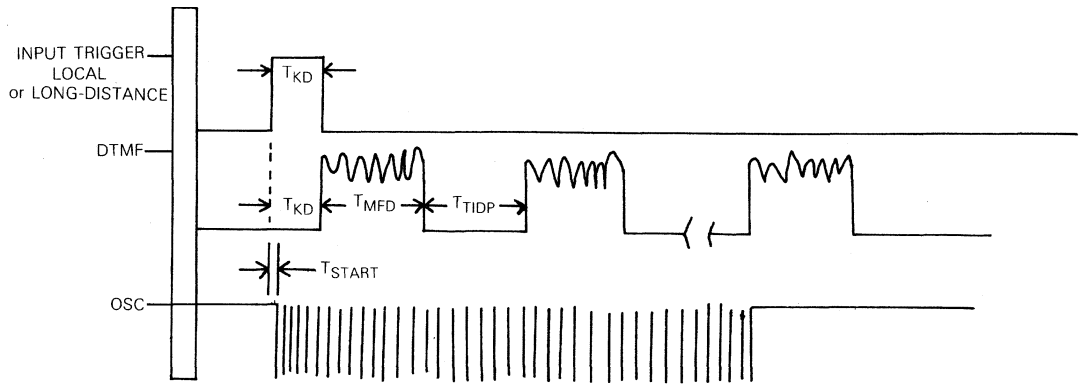


Figure 3: Waveforms

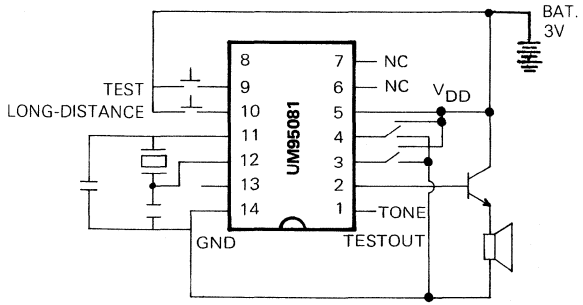
Telephone Number Selection Table (UM95081)

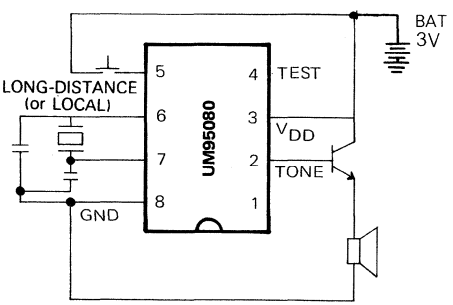
S1	S2	Local	Long-Distance	Comment
V_{DD}	V_{DD}	⊓		1st local number
V_{DD}	V_{DD}		⊓	1st long-distance number
V_{SS}	V_{DD}	⊓		2nd local number
V_{SS}	V_{DD}		⊓	2nd long-distance number
V_{DD}	V_{SS}	⊓		3rd local number
V_{DD}	V_{SS}		⊓	3rd long-distance number
V_{SS}	V_{SS}	⊓		4th local number
V_{SS}	V_{SS}		⊓	4th long-distance number

Timing Diagram



Application Circuits

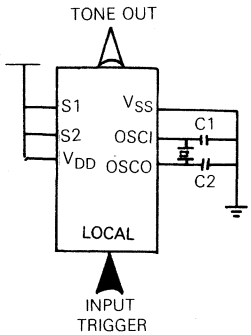




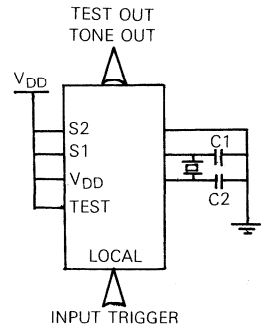
Note: It is suggested that the tone amplitude used be as small as possible in order to reduce distortion when the tone enters the handset transmitter.

Test Circuits

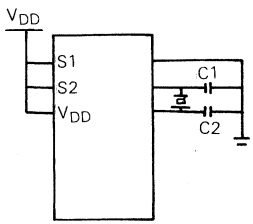
A)



C)



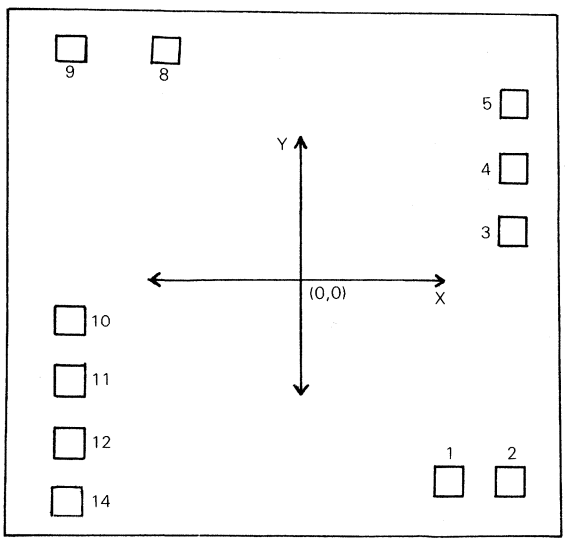
B)



Bonding Diagram

Chip size 85 X 82 mils

Thickness: 15 Mils



Unit: um

Pad No.	Designation	X	Y
1	TEST OUT	480	−860
2	TONE	840	−840
3	S1	820	100
4	S2	820	340
5	V_{DD}	820	560
8	TEST	−620	840
9	LOCAL	−860	840
10	LONG-DISTANCE	−880	−140
11	OSCI	−880	−400
12	OSCO	−880	−640
14	GND	−880	−860

Placing Orders:

Customers who wish to order the UM95080/81 must complete an ordering information form (Table 1) and submit this information to UMC along with their first order. UMC will assign a specific version number for each individual product and inform customers of their particular version number. Reorders can then be made by noting only the part (UM95080/UM95081) and version numbers.

Table 1

Part No.:	☐ UM95081		☐ UM95080
Form:	☐ Chip		☐ Package
Stored Phone Numbers	Input Trigger (local or long distance)	S1 (UM95081 only)	S2 (UM95081 only)

Design and Production Process

Samples for customer verification and approval will be available five weeks after UMC receives a customer's order and order information form (see Table 1 and Figure 4). After samples are verified and approved by customers, another two weeks will be necessary for production of the complete order and shipment. Assuming no unforessen difficulties, the overall production schedule for filling orders on the UM95080/81 should take about seven weeks.

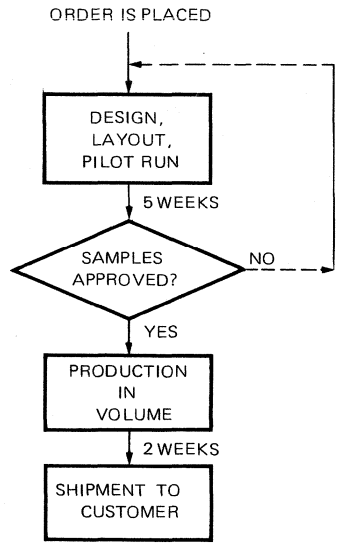


Figure 4: Ordering Procedure and Production Flow

UM95087

Tone Dialer

Features

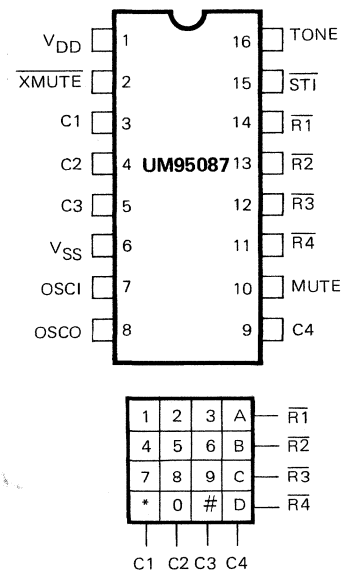
- Direct replacement for Mostek MK5087
- Operating voltage range: 3.5 to 10.0 Volts
- Uses 3.58 MHz TV crystal to derive all frequencies, providing high accuracy and stability
- On-chip regulation of dual and single-tone amplitudes
- Built-in auxiliary switching functions
- Built-in mute driver
- Minimum external parts count
- Multiple key entry is pin selectable for either single tone or no tone

General Description

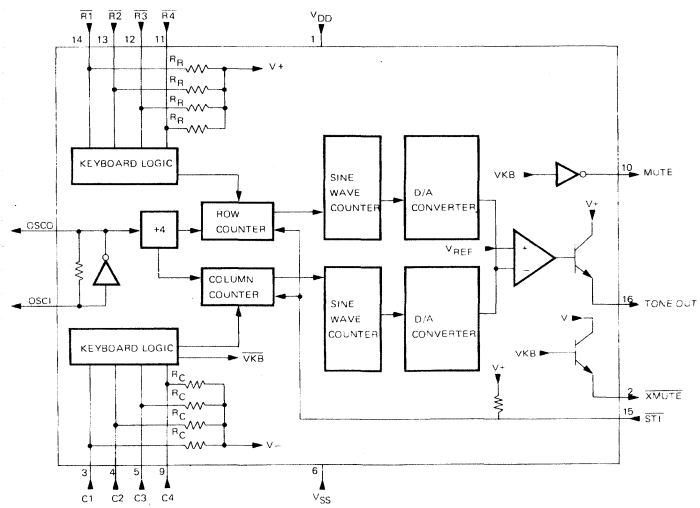
The UM95087 is a monolithic CMOS integrated circuit designed for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The UM95087 was designed specifically for performance. Its features include single contact static keyboard input; single-tone inhibit ($\overline{STI}$) option; wide supply voltage operation with regulated output. The UM95087 provides high performance with low output tone distortion: THD < −20dB.

Pin Configuration & Keyboard Assignments



Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage . . . . . −0.3V to V
Input Voltage . . . . . −0.3V to V_{DD} + 0.3V
Maximum Power Dissipation . . . . . 500 mW
Operating Temperature . . . . . −20°C to +70°C
Storage Temperature . . . . . −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (T_{OP} = 25°C, F_{OSC} = 3.579545 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		Test Ckt.
Operating Voltage	V_{DD}	3.5		10	V			B
Supply Operating Current	I_{DD1}		1.0	2.0	mA	V_{DD} = 3.5V	All outputs unloaded	B
	I_{DD2}		13	20	mA	V_{DD} = 10.0V	Oscillator running	
Standby Current	I_{SD1}		0.2	100	μA	V_{DD} = 3.5V	All outputs unloaded	A
	I_{SD2}		0.3	200	μA	V_{DD} = 10.0V	Oscillator not running	
$\overline{XMUTE}$ Output Current	I_{OH1}	−15	−25		mA	V_{DD} = 3.5V, V_{OH} = 2.5V, No key entry		C
	I_{OH2}	−20	−31		mA	V_{DD} = 10.0V, V_{OH} = 8.0V, No key entry		
XMTR Output Leakage Current	I_{OL1}		0.1	100	μA	V_{DD} = 10.0V, V_{OL} = 0.0V, with key entry		C
MUTE Output Drive Current	I_{OH1}	−0.5	−0.8		mA	V_{DD} = 3.5V, V_{OH} = 3V, with key entry		C
	I_{OH2}	−1	−4.5		mA	V_{DD} = 10.0V, V_{OH} = 9.5V, with key entry		
MUTE Output Sink Current	I_{OL1}		3.0		mA	V_{DD} = 3.5V, V_{OL} = 0.5V, No key entry		C
	I_{OL2}		7.5		mA	V_{DD} = 10.0V, V_{OL} = 0.5V, No key entry		
Row Input Current	I_R	100	175		μA	V_{IN} = 0V, All outputs unloaded		—
Column Input Current	I_C	100	140		μA	V_{IN} = 3.5V, All outputs unloaded		—
Input Voltage Range	V_{IH}	0.8	V_{DD}		V_{DD}	-		—
	V_{IL}		0	0.2	V_{DD}			
Single Column Tone Output Amplitude	V_{OC}	396	500	630	mV_{P-P}	R_L = 1 KΩ, V_{DD} = 3.5V		B
		396	500	630		R_L = 1 KΩ, V_{DD} = 10.0V		
Single Row Tone Output Amplitude	V_{OR}	317	400	504	mV_{P-P}	R_L = 1 KΩ, V_{DD} = 3.5V		B
		317	400	504		R_L = 1 KΩ, V_{DD} = 10.0V		
Pre-Emphasis	T_{WIST}	1.0	2.0	3.0	dB			B
Valley of Single Tone	V_V	0.23	3.0		V_{DD}			B
Distortion	DIS%			10	%	V_{DD} = 5 * Note		B
Tone Output External Load Impedance	R_L	620			Ω	V_{DD} = 3.5V		—
		330			Ω	V_{DD} = V		
$\overline{STI}$ Input Resistance	R_{IN}	20	40	100	KΩ	25°C		—

*Note: $$DIS(\%) = \frac{100(V_1^2 + V_2^2 + \ldots + V_n^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$$

(a) $V_1 \ldots V_n$ are the intermodulation or harmonic frequencies in the 500 Hz to 3400 Hz band.

(b) V_{IL} and V_{IH} are the individual frequency components of the DTMF signal.

AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Tone Output Rise Time	T_R			8.5		ms
OSC Startup Timing	T_{START}			8		ms
Predigital Pause	T_{TPDP}			5		ms
Mute Delay	T_{MOT}			5		ms

R/C	Condition	Spec.	Actual	Error (%)	Unit
$\overline{R1}$	F_{OSC} = 3.579545 MHz	697	701.3	+0.62	HZ
$\overline{R2}$		770	771.4	+0.19	HZ
$\overline{R3}$		852	857.2	+0.61	HZ
$\overline{R4}$		941	935.1	–0.63	HZ
C1		1,209	1,215.9	+0.57	HZ
C2		1,336	1,331.7	–0.32	HZ
C3		1,477	1,471.9	–0.35	HZ
C4		1,633	1,645.0	+0.73	HZ

% Error does not include oscillator drift

Pin Description

Pin	Designation	Description
1 6	V_{DD} V_{SS}	Power supply. These are the power supply input pins. The UM95087 is designed to operate from 3.5 to 10.0 volts.
2	$\overline{XMUTE}$	$\overline{XMUTE}$ switch output. This pin is connected to the emitter of an on-chip bipolar transistor whose collector is connected to V_{DD}. With no keyboard input, this transistor is turned on and pulls the pin up to within V_{BE} of the V_{DD} supply. When a keyboard entry is sensed, this output goes open circuit (high impedance). The XMTR switch output switches regardless of the state of the $\overline{STI}$ pin input.
3 4 5 9 14 13 12 11	C1 C2 C3 C4 $\overline{R1}$ $\overline{R2}$ $\overline{R3}$ $\overline{R4}$	Keyboard inputs. The UM95087 features inputs compatible with the standard 2-of-8 keyboard (the inexpensive single-contact Form A keyboard). No noise is generated by scanned or dynamic input. Normal operation with a keyboard produces dual tone generation when a single button is pushed. A single tone is generated when two or more buttons in the same row are pushed. Pushing two buttons diagonal to each other will result in no tone being generated. When the push of a button produces input to a single row and column, the tone for a digit is generated. Input to two buttons in a single column will produce a column tone. Input to more than one column will not produce any tone. The internal circuit of the UM95087 will not sense the activation of a single row. If a single-row tone is desired, two columns in the desired row must be activated.

Pin Description (Continued)

Pin	Designation	Description
7 8	OSCI OSCO	Oscillator input/output. The UM95087 contains an on-chip inverter with sufficient loop gain to provide oscillation when working with a low cost television color-burst crystal. The circuit is designed to work with a 3.579545 MHz crystal. The oscillator is disabled whenever a keyboard input is absent. Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ±0.02%.
10	MUTE	MUTE output. The MUTE output is a conventional CMOS gate that pulls to V_{SS} with no keyboard input and pulls to V_{DD} supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The MUTE output switches regardless of the state of $\overline{STI}$ pin input.
15	$\overline{STI}$	Single tone inhibit input. The $\overline{STI}$ input is used to inhibit the generation of other than dual tones. It has a pull-up to V_{DD} and when left floating or tied to V_{DD}, single or dual tones may be generated. When forced to V_{SS}, any input situation that would result in a single tone will now result in no tone, but all other chip functions will operate normally.
16	TONE	DTMF signal output. The TONE OUT is connected internally in the UM95087 to the emitter of an NPN transistor and is the on-chip operational amplifier which mixes the row and column tones together.

Functional Description

1. Keyboard

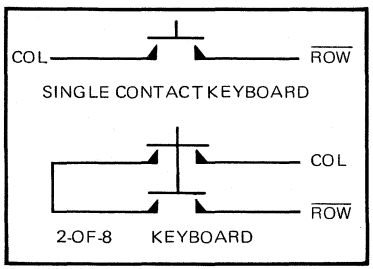


Figure 1 Keyboard Configurations

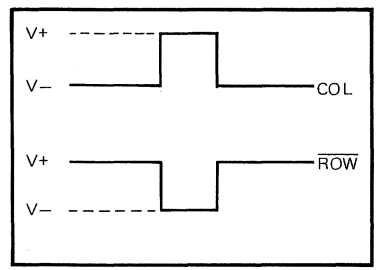


Figure 2 Electrical Inputs

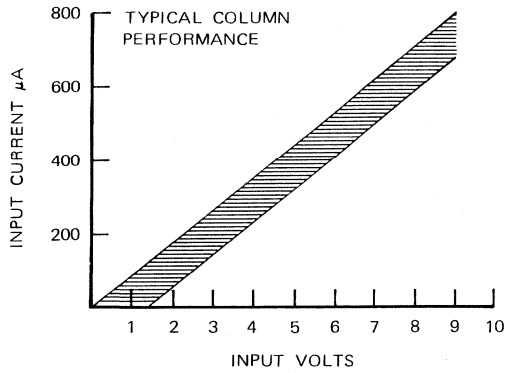


Figure 3 Typical Input Operating Conditions for Pins 3, 4, 5 and 9 with Voltage Reference V_{SS} @ 25°C.

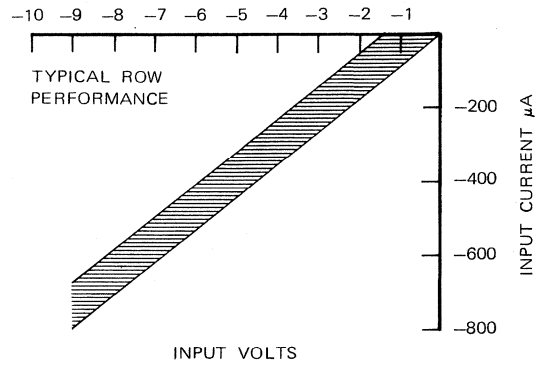


Figure 4 Typical Input Operating Conditions for Pins 11, 12, 13, & 14 with Voltage Reference V_{DD} @ 25°C.

2. Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for the generation of tones. The tolerance specification can be relaxed as follows:

Frequency: 3.58 MHz ± 0.02%.
R_S < 100 Ω, L_M = 96mH, C_M = 0.25pF, C_H = 5pF, C_L = 18pF.

3. The DTMF Generator

The Row and Column output waveforms are shown in Figures 5 and 6 below. In the UM95087, these waveforms are digitally synthesized using on-chip D to A converters, and are provided with output level regulation. The maximum THD of the dual tone is −20dB.

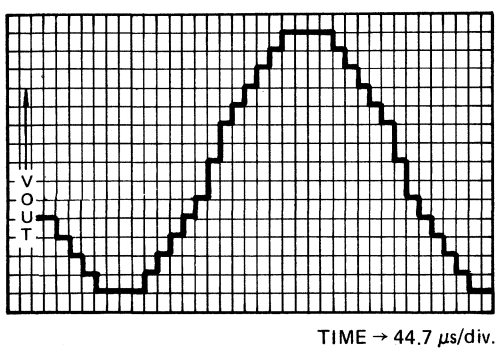


Figure 5 Single Row Output Waveform

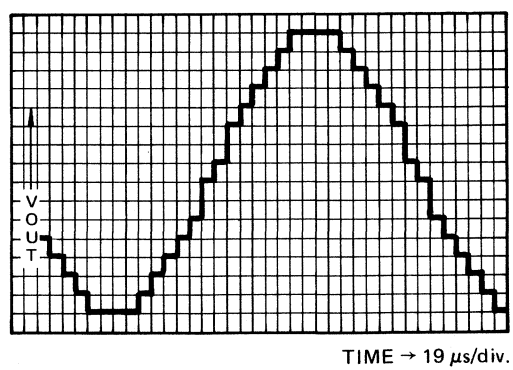
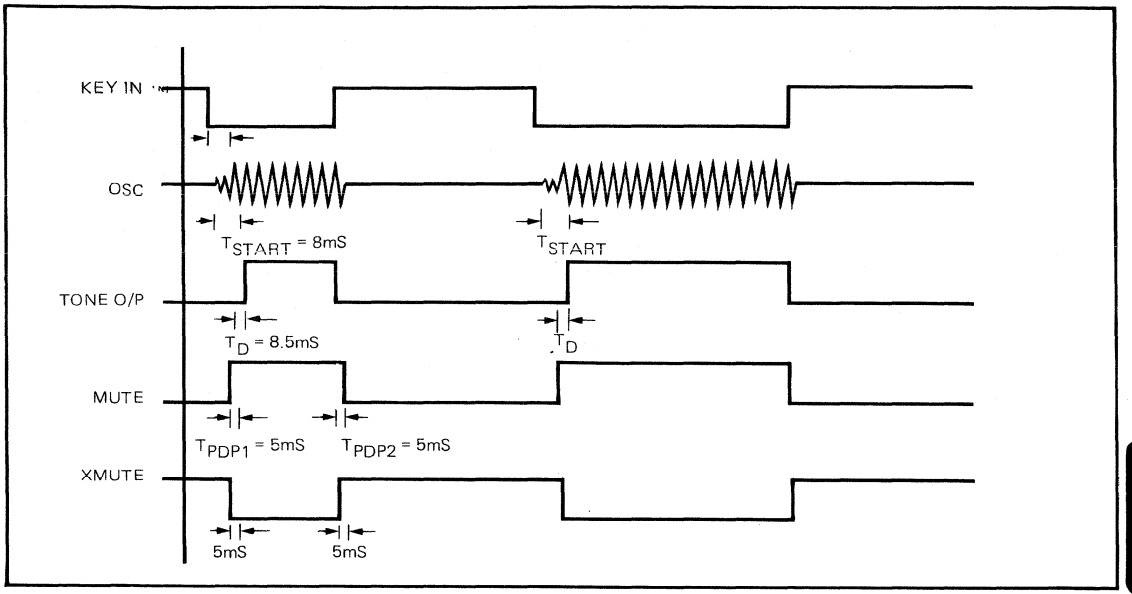
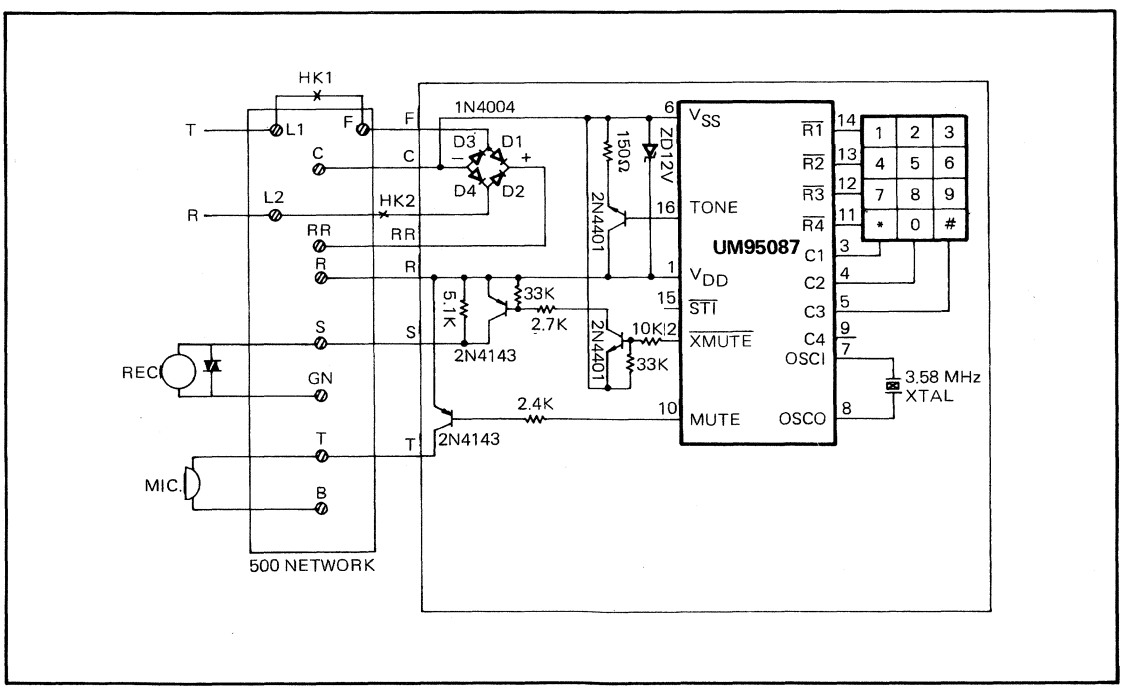


Figure 6 Single Column Output Waveform

Timing Diagram

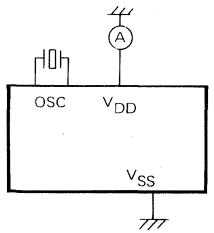


Application Circuit

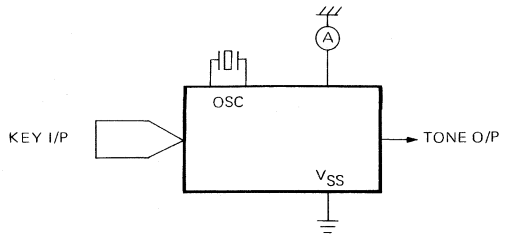


Test Circuits

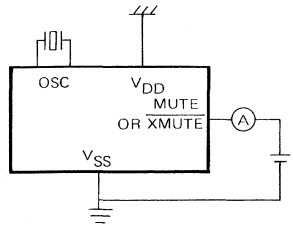
(A)



(B)



(C)



UMC

UM95088

Tone Dialer

Features

- Wide supply voltage range: 1.8V to 5.5V
- Ceramic oscillator (480K ceramic resonator)
- Fully debounced scanning keyboard
- Minimum tone duration: 73 ms
- Very low tone distortion: less than 1% in band
- On-chip power-on reset
- Single-tone output mode
- Low standby and operating power
- All pins protected against ESD and latch-up
- Low frequency error: max. +0.3%

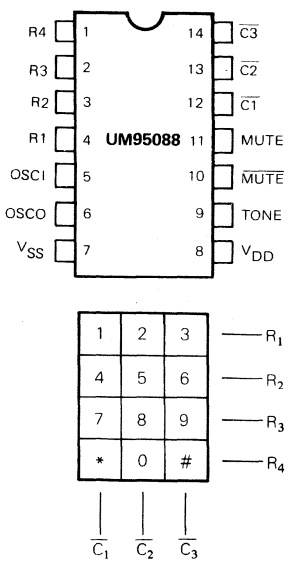
General Description

The UM95088 DTMF is specifically designed to implement a dual tone telephone dialing system in applications which require a fixed supply operation and a highly stable tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard XY matrix telephone keyboard and operates directly from the telephone lines.

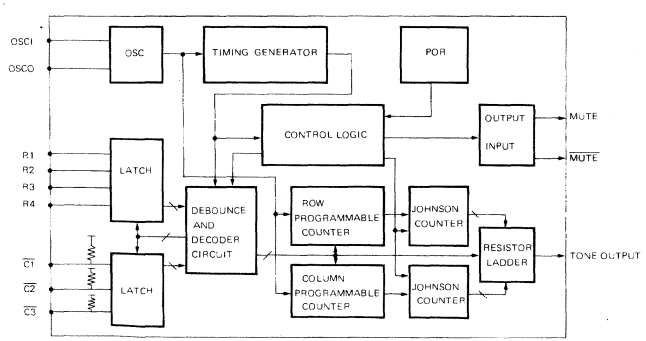
All the required dual-tone frequencies are derived from the widely used 480 KHz ceramic resonator, which provides high accuracy and stability. The sinusoidal waveforms for the individual tones are digitally synthesized on the chip. Waveforms so generated have low total harmonic distortion.

The built-in minimum tone duration function provides an adaptive solution and fast dialing with short DTMF output is achieved. A reliable power-on reset circuit guarantees proper functioning under a variety of power supply conditions.

Pin Configuration & Keyboard Assignments



Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage . . . . . −0.3V to +6.0V
Input Voltage . . . . . −0.3V to V_{DD} + 0.3V
Maximum Power Dissipation 500mV
Operating Temperature . . . . . −20°C to +70°C
Storage Temperature . . . . . −55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 480 KHz, T_{OP} = 25°C, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	Test CKT.
Operating Voltage	V_{DD}	1.5		5.5	V	OSC Running, All O/P Unloaded	B
Operating Current	I_{DD}	0.35	0.4	0.5	mA	V_{DD} = 2.0V, All O/P Unloaded	B
Standby Current	I_{SD1}		3.0	4.5	μA	V_{DD} = 2.0V, All O/P Unloaded	A
	I_{SD2}		5.0	6.0	μA	V_{DD} = 3.5V, All O/P Unloaded	A
MUTE Output Sink Current	I_{OL1}	0.5	0.7		mA	V_{DD} = 2.0V, V_{OL} = 0.5V	C
	I_{OL2}	1.0	1.7		mA	V_{DD} = 3.5V, V_{OL} = 0.5V	C
MUTE Output Source Current	I_{OH1}	0.3	0.45		mA	V_{DD} = 2.0V, V_{OH} = 1.5V	C
	I_{OH2}	0.7	0.9		mA	V_{DD} = 3.5V, V_{OH} = 3.0V	C
$\overline{MUTE}$ Output Sink Current		0.5	0.7		mA	V_{DD} = 2V, V_{OL} = 0.5V	C
		1.0	1.3		mA	V_{DD} = 3.5V, V_{OL} = 0.5V	C
$\overline{MUTE}$ Output Source Current		0.5	0.9		mA	V_{DD} = 2V V_{OH} = 1.5V	C
		2	4		mA	V_{DD} = 3.5V V_{OH} = 3.0V	C
Row I/P Current			0.65		mA	V_{DD} = 3.5V, V_{IN} = 0V	—
Column I/P Current			16.5		μA	V_{DD} = 3.5V, V_{IN} = 0V	—
Input Voltage Range	V_{IH}	0.8V_{DD}		1	V_{DD}		—
	V_{IL}	0		0.2	V_{DD}		—
Single Column Tone Output Amplitude	V_{OC1}	500	560	600	mV	V_{DD} = 2.0V, R_{LOAD} = 15KΩ	B
	V_{OC2}	850	1000	1100	mV	V_{DD} = 3.5V, R_{LOAD} = 15KΩ	B
Single Row Tone Output Amplitude	V_{OR1}	360	420	480	mV	V_{DD} = 2.0V, R_{LOAD} = 15KΩ	B
	V_{OR2}	650	750	780	mV	V_{DD} = 3.5V, R_{LOAD} = 15KΩ	B
Valley of Single Tone	V_V	0.30	0.36	0.45	V_{DD}	R_{LOAD} = 15KΩ	B
Distortion	T_{HD}			5.0	%	Note*	B
Pre-emphasis	Twist	1	2	3	dB		B

Note: $$DIS(\%) = \frac{100X(V_1^2 + V_2^2 + \ldots + V_n^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$$

(a) $V_1 \ldots V_n$ are the intermodulation or harmonic frequencies in the 500 Hz to 3,400 Hz band.
(b) V_{IL} and V_{IH} are the individual frequency components of the DTMF signal.

AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
OSC Start up Time	T_{START}	V_{DD} = 2.0 ~ 5.5V		5		mS
Debounce Time	T_D			10		mS
Minimum Tone Duration	T_{MTD}			73		mS
Pre-Digit Pause	T_{PDP1}			43		mS
Mute Delay Time	T_{PDP2}			5		mS
Inter-digit pause	T_{TIDP}			73		mS

Comparisons of Specified vs. Actual Tone Frequencies.

Table 1 shows the frequency tolerance of the output tones for DTMF signals generated by the UM95088 tone output pin.

Output Frequency (Hz)			% Error*
Specified		Actual	
697	(Row 1)	695.65	–0.19
770	(Row 2)	769.23	–0.10
852	(Row 3)	851.06	–0.11
941	(Row 4)	941.18	+0.02
1,209	(Column 1)	1,212.12	+0.26
1,336	(Column 2)	1,333.33	–0.20
1,477	(Column 3)	1,481.48	+0.30

* : % Error does not include oscillator drift

Table 1

Pin Description

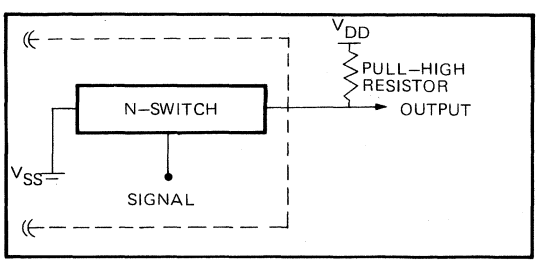
Pin	Designation	Description
1,2,3,4 12,13,14	R4 to R1 $\overline{C1}$ to $\overline{C3}$	Key inputs These are the keyboard input pins of the UM95088. The output of the Column pins, $\overline{C1}$, $\overline{C2}$ and $\overline{C3}$ are high and the output of the Row pins, R1, R2, R3 and R4 are low in the standby state. Each column has a pull-up resistor (120 KΩ typically). A logic low is presented at the connected row and column pins. A debouncing circuit is provided (10 ms typically). Multiple keys – Single Tone output is provided for testing purposes.

Pin Description (Continued)

Pin	Designation	Description
5 6	OSCI OSCO	Oscillator input/output A 480 KHz ceramic resonator and two 100pF serial loading capacitors form a complete oscillator circuit. The oscillator circuit is activated upon the depression of any key. Maximum start up time is 5 mS at V_{DD} = 3.5V
7 8	V_{SS} V_{DD}	Power supply V_{SS}: Negative Power Supply V_{DD}: Positive Power Supply Operating Voltage Range is 1.8V to 5.5V.
9	TONE	Dual-tone multi-frequency signal output The output impedance is typically 1.5 KΩ. This pin is forced to V_{SS} when there is no output. The column tone to row tone ratio is typically 2 dB. A single tone is created by pressing two or more keys in a row for the appropriate row tone and two or more keys in a column for the appropriate column tone.
10	$\overline{\text{MUTE}}$	MUTE signal output active low This is an open drain output device. This output is activated during tone output. It can sink the current from a higher voltage source (> V_{DD}) directly.
11	MUTE	MUTE signal output active high This is an inverter output. The output is activated during tone output. The source/sink capability is 0.45/0.7 mA at 2V supply voltage and 0.5 drain voltage fall.

Functional Description:

1. N-Channel Open Drain Output – MUTE



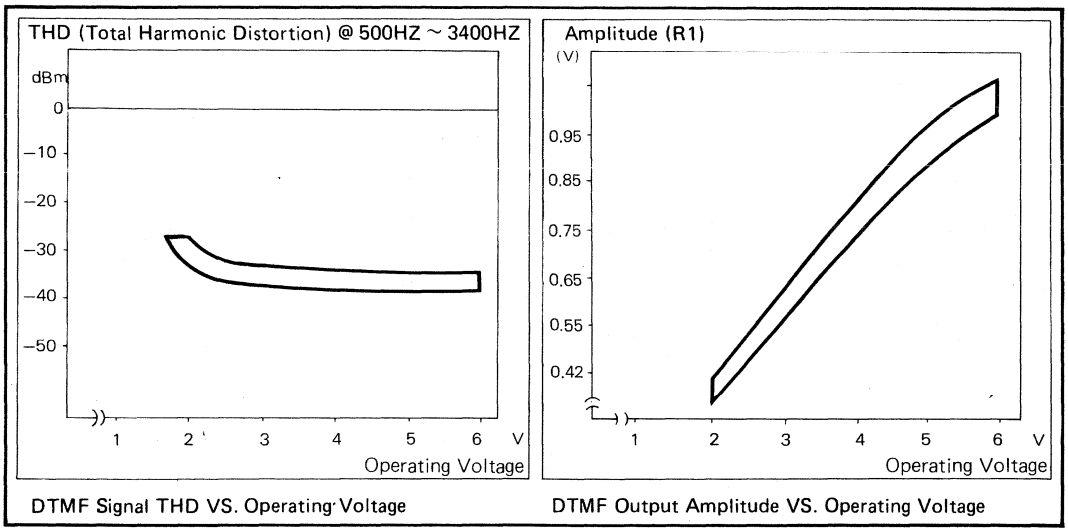
DTMF Tone Generator

The UM95088 is well designed with a 6 level, 12 segment, 1/2 V_{DD} reference voltage structure. The Total Harmonic Distortion (THD) of the UM95088 DTMF output is typically 5%, which is a very low value compared with the EIA RS-470 standard of 10% THD.

The temperature coefficient of the DTMF output amplitude is balanced to zero from the adaptive DTMF generator structure. The output strength of the Column Tone is pre-emphasized 2.5 dB higher than the Row Tone.

The typical equivalent output impedance of the DTMF generator is 1.5 KΩ.

"Single tone O/P vs. operating voltage" and "DTMF output amplitude vs. operating voltage" is shown in figures 1 and 2 for reference in circuit design.

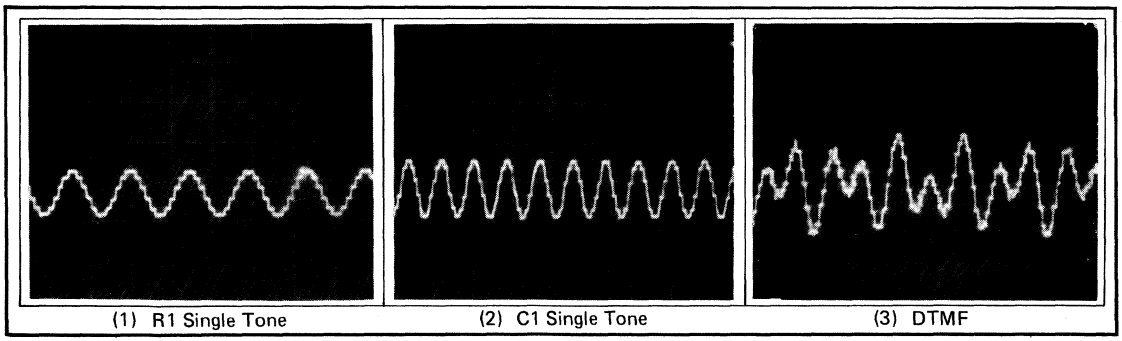


DTMF Signal THD VS. Operating Voltage

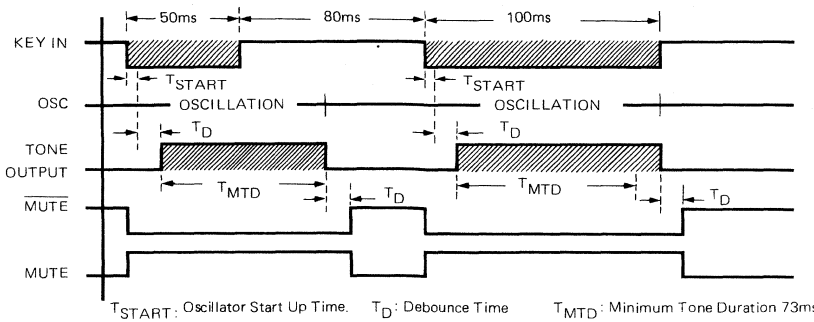
Figure 1

DTMF Output Amplitude VS. Operating Voltage

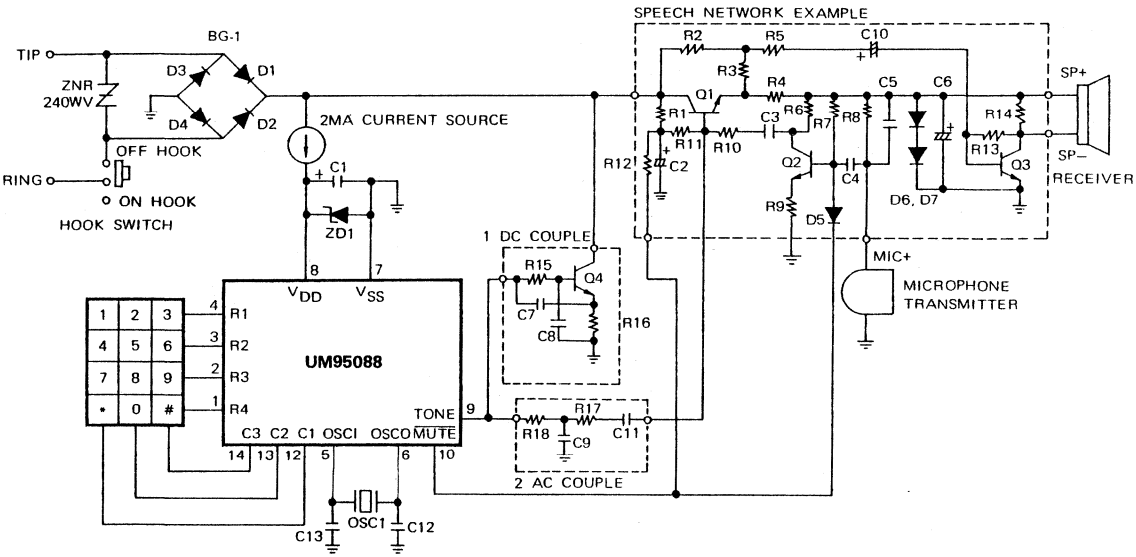
Figure 2



Timing Diagram (when power supply is ready)



A Low Cost Touch-Tone Telephone Application



Parts List

Diode

$D_1 \sim D_4$: IN4004 x 4
D_5, D_6, D_7: IN4148 x 3

Transistor

$Q_1 \sim Q_4$: 2SC945 x 4

Resistor:

R1 : 4K7
R2 : 3K3
R3 : 180Ω
R4 : 22Ω
R5 : 1K2
R6 : 1K2
R7 : 680K
R8 : 2K2
R9 : 75Ω
R10: 4K7
R11: 22K
R12: 10K
R13: 10K
R14: 1K2
R15: 1K2
R16: 220Ω
R17: 10K
R18: 1K2

Capacitor

C1 : 10μF/16WV
C2 : 10μF/16WV
C3 : 0.1μF/50WV
C4 : 0.033μF/50WV
C5 : 0.033μF/50WV
C6 : 47μF/10WV
C7 : 0.033μF/50WV
C8 : 0.033μF/50WV
C9 : 0.0033μF/50WV
C10: 1μF/10WV
C11: 0.033μF/50WV
C12: 100PF
C13: 100PF

Oscillator

OSCI: 480KHz Ceramic Resonator

High Voltage Protector

ZNR: 240WV/1W Varistor

Zener Diode

ZDI: 3.9WV/0.5W ZD

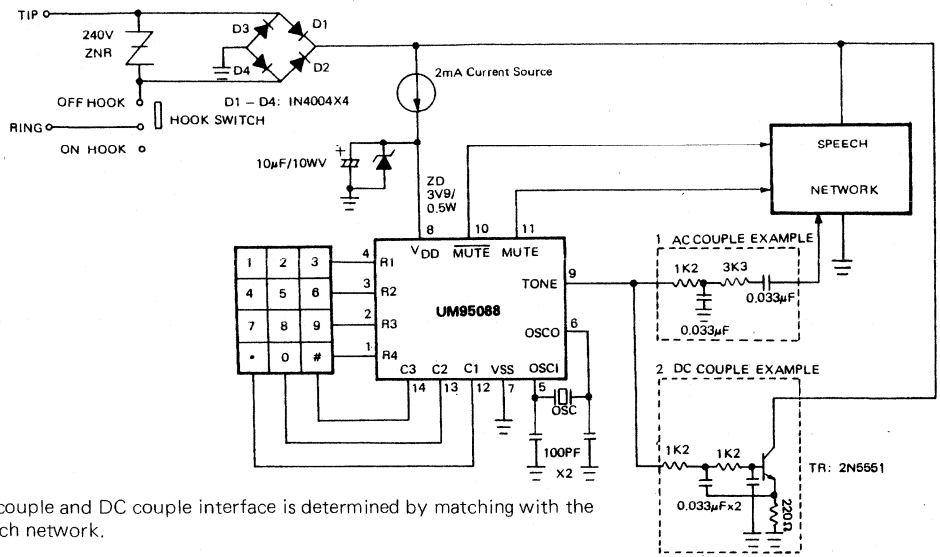
Receiver

100 OHM receiver

Transmitter

ECM mic.

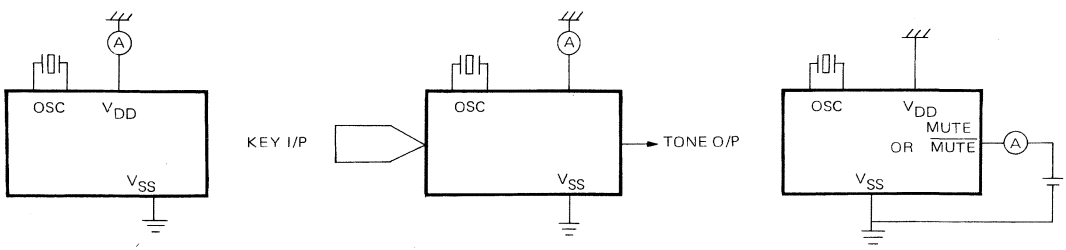
Touch Tone Telephone Application



Note: AC couple and DC couple interface is determined by matching with the speech network.

Test Circuits

(A) (B) (C)



UMC

UM95089
Tone Dialer

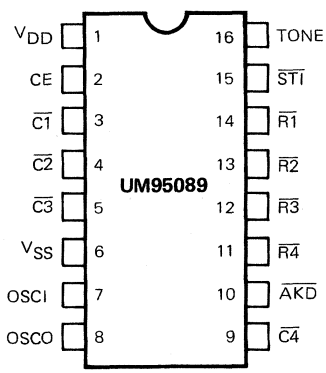
Features

- Wide operating voltage range: 2.5 to 10 volts.
- Optimal for use with a constant operating supply voltage (3.5V typically).
- Tone amplitude stability of ± 1.5dB within the suggested operating temperature range.
- Device power may be derived directly from telephone lines or from small batteries.
- TV crystal standard (3.58 MHz) is used to derive all frequencies, providing high accuracy and stability.
- Specifically designed for electronic telephone applications.
- Interfaces directly to a standard push-button telephone keyboard with common terminal.
- Low total harmonic distortion.
- Dual tone/single tone capability.
- Can be used as a direct replacement for AMI S25089 and Mostek MK5089 tone generators.

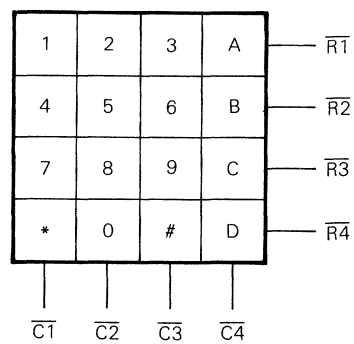
General Description

The UM95089 DTMF generator is specifically designed for applications requiring a fixed supply operating voltage and a high stability tone output, making it ideal for electronic telephone applications. The UM95089 interfaces directly to a standard push-button telephone keyboard (common terminal connected to VSS) and operates directly from telephone lines. All necessary dual-tone frequencies are derived from the widely-used TV crystal standard, providing high accuracy and stability. The required sinusoidal waveform for individual tones is digitally synthesized on the chip, resulting in a waveform with low total harmonic distortion. A voltage reference which is stable over the operating temperature range is generated on the chip; this reference is used to regulate the dual tone frequency levels to ensure that they meet recommended telephone industry specifications.

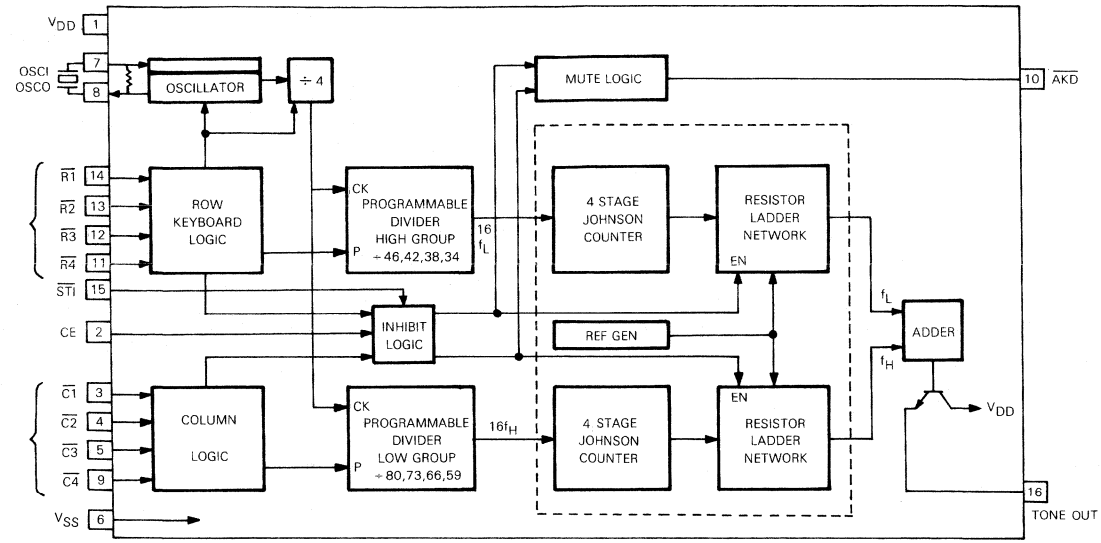
Pin Configuration



Keyboard Assignments



Block Diagram



Absolute Maximum Ratings *

Power supply voltage (V_{DD}-V_{SS})..... −0.3 to +10.5V.
Input voltage (V_{IN})..... −0.3 to V_{DD}+0.3V.
Maximum power dissipation (at 25°C).....500 mW.
Operating temperature (T_{OP})..... −20°C to +70°C.
Storage temperature (T_{STG})..... −55°C to +150°C.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(T_{OP}=25°C, F_{OSC}=3.579545 MHz unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD1}	2.5		10	V	Valid key input (tone output mode)	B
	V_{DD2}	1.6		10	V	$\overline{AKD}$ outputs vary with key input (non-tone output mode)	
Supply Operating Current	I_{DD1}		1.0	1.4	mA	V_{DD}=3V, one key input, all outputs unloaded	B
	I_{DD2}		6.6	10	mA	V_{DD}=10V, one key input, all outputs unloaded	
Standby Current	I_{SD1}		1	20	μA	V_{DD}=3V, no key input, all outputs unloaded	A
	I_{SD2}		5	100	μA	V_{DD}=10V, no key input, all outputs unloaded	
$\overline{AKD}$ Output Sink Current	I_{OL}	0.5	1		mA	V_{DD}=3V, V_{OL}=0.5V	C

DC Characteristics (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
$\overline{AKD}$ Output off Leakage Current	I_{OH}		1	10	μA	V_{DD}=10V	C
Input Voltage Range	V_{IH}	0.8		1	V_{DD}		—
	V_{IL}	0	9	0.2	V_{DD}		
Row & Column Input Current (Pull-up)	I_{IH}	30	90	150	μA	V_{DD}=3V, V_{IH}=0V	—
	I_{IH}	100	300	500	μA	V_{DD}=10V, V_{IH}=0V	—
Single Column Tone Output Amplitude	V_{OC}	760	830	900	mVp-p	V_{DD}=2.5V, R_L=10Kohm	B
		2028	2200	2380	mVp-p	V_{DD}=10V, R_L=100Kohm	
Single Row Tone Output Amplitude	V_{OR}	550	600	650	mVp-p	V_{DD}=2.5V, R_L=10Kohm	B
		1520	1650	780	mVp-p	V_{DD}=10V, R_L=100Kohm	
Pre-Emphasis	Twist	1	2	3	dB		B
Distortion	DIS%		1	5	%	V_{DD}=5V, *Note	B
Oscillator Output Drive Current	I_{OH1}	0.13	0.31		mA	V_{DD}=3V, V_{OH}=2.5V, one key input	C
	I_{OH2}	0.42	1.1		mA	V_{DD}=10V, V_{OH}=9.5V, one key input	C
Oscillator Output Sink Current	I_{OL1}	0.21	0.52		mA	V_{DD}=3V, V_{OL}=0.5V, one key input	C
	I_{OL2}	0.8	2.1		mA	V_{DD}=10V, V_{OH}=0.5V, one key input	C
Input/Output Capacitance	CI/01		12	16	pF	V_{DD}=3V	—
	CI/02		10	14	pF	V_{DD}=10V	—

Note: DIS (%) $= \dfrac{100(V_1^2 + V_2^2 + \ldots\ldots + Vn^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$

where 1. $V_1 \ldots Vn$ are the intermodulation or harmonic frequencies in the 500 Hz to 3400 Hz band, and
2. V_{IL}, V_{IH} are the individual frequency components of the DTMF signal.

AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start up Time	T_{START}		2	5	ms	V_{DD}=3.0~10.0V
Tone Output Rise Time	T_R		2	5	ms	
Pre-Digit Pause	T_{PDP}		0	0	ms	

R/C	Condition	Spec.	Actual	Error %	Unit
R1	F_{OSC} = 3.579545 MHz	697	699.2	+ 0.32	Hz
R2		770	766.27	− 0.48	Hz
R3		852	847.54	− 0.64	Hz
R4		941	948.09	− 0.75	Hz
C1		1209	1216	+ 0.58	Hz
C2		1336	131.8	− 0.33	Hz
C3		1477	1472	− 0.34	Hz
C4		1633	1645	+ 0.73	Hz

Pin Description

Pin	Designation	Description
1 6	V_{DD} V_{SS}	Positive power supply input. Negative power supply input. The UM95089 is designed to operate within a range of 2.5 to 10.0 volts.
2	CE	Chip enable input. The chip enable input has an internal pullup to V_{DD}. When this input is left unconnected or connected to V_{DD}, the UM95089 operates normally. When this input is connected to V_{SS}, tone generation is inhibited; all other chip functions continue to operate normally, however.
3—5, 9 11—14	$\overline{C1}$ ~ $\overline{C4}$ $\overline{R4}$ ~ $\overline{R1}$	Keyboard inputs. Internal pullup resistors are present on the row and column inputs (20Kohm — 10Kohm); low levels on a particular row and column input correspond to a key entry. The UM95089 interfaces with the standard push-button telephone keyboard (see Figure 1). (Keyboard common terminal must be connected to V_{SS}.)
7 8	OSCI OSCO	Oscillator input. Oscillator output. The UM95089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip, making it necessary to connect only a standard 3.58Mhz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator is enabled whenever a row input is activated.
10	$\overline{AKD}$	Any key down output. The $\overline{AKD}$ output consists of an open drain N-channel device. When no keys are pressed, the $\overline{AKD}$ output is open. When a key is pressed, the $\overline{AKD}$ output = V_{SS}.

Pin Description (Continued)

Pin	Designation	Description
15	$\overline{STI}$	Single tone inhibit input. The $\overline{STI}$ input is used to inhibit generation of tones other than dual tones. It has an internal pull-down to V_{SS}. When this input is left unconnected or connected to V_{SS}, the single tone mode is disabled. When this input is connected to V_{DD}, single as well as dual tones may be generated as follows: Dual tone mode: When one row and one column are selected, a dual tone output consisting of an appropriate low group tone and high group tone is generated. If two digit keys that are not in the same row or same column are pressed, the dual tone mode is disabled and no output is provided. Single tone mode: Low group tones can be generated by pressing two digit keys in the appropriate row. High group tones can be generated by pressing two digit keys in the appropriate column, i.e. selecting the appropriate column input and pressing two row inputs in that column.
16	TONE	DTMF signal output. The UM95089 uses a Johnson counter and resistor ladder network (see block diagram) to synthesize the two desired frequencies in sinewaves. The ladder network is then used to mix the two. The UM95089 uses a bipolar NPN transistor, connected as emitter follower, to allow proper impedance transformation and at the same time preserve signal level.

Functional Description

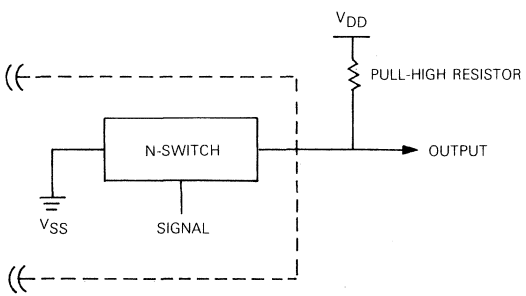
Crystal Specification

Standard TV color burst crystals have a much tighter tolerance specification than is necessary for tone generation applications. Because the required tolerance specification for this type of application is more relaxed, lower-cost crystals can be used. Crystals with the following specifications are suggested for use with the UM95089:

Frequency: 3.58 MHz ± 0.02%.

$R_S \leq 100$ohm, L_M = 96 mH, C_M = 0.02pF, C_H = 5pF, C_L = 12pF.

$\overline{AKD}$ Output Structure



N-CHANNEL OPEN DRAIN OUTPUT

DTMF Generator

The UM95089 has a well designed, digitally-synthesized sinewave with an 8-level, 16-segment structure. (See Figure 2.)

Reference Voltage

The structure of the reference voltage employed in the UM95089 is shown in Figure 3. It has the following characteristics:

a) V is proportional to the supply voltage. Output tone amplitude, which is a function of ($V_{DD} - V_{REF}$), increases with supply voltage. (Figure 4).

b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistor divider also contributes to providing an accuracy of better than 10%. As a result, tone amplitude variations over temperature and unit to unit differences are held to less than ± 1.0dB.

c) Resistor values in the divider network are chosen so that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. This eliminates tone output clipping at low supply voltage and improves distortion performance.

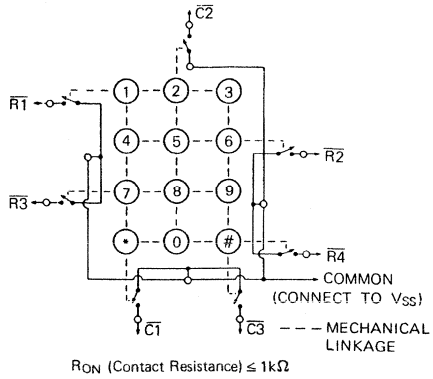


Figure 1. Standard Telephone Push-Button Keyboard

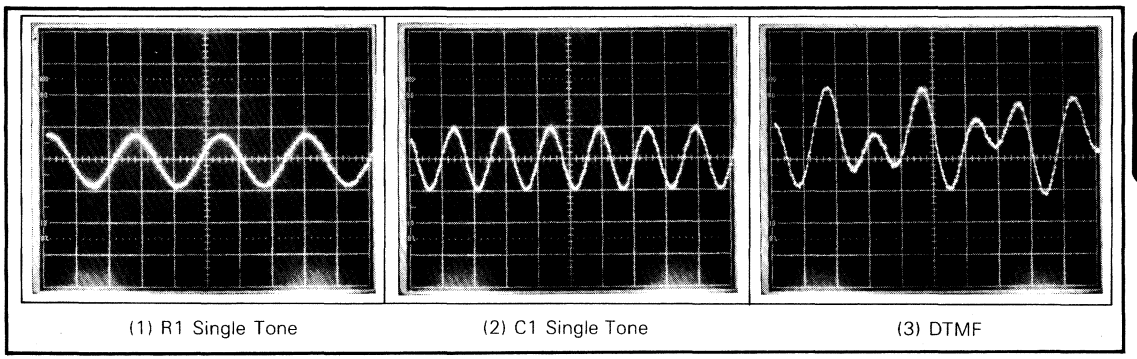


Figure 2. Waveforms

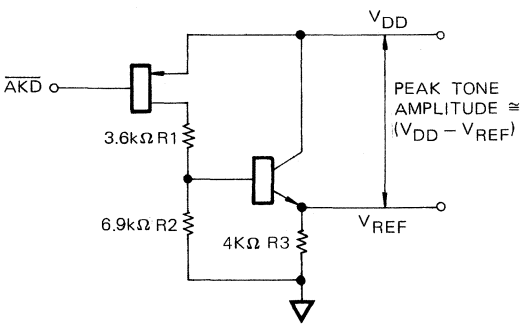


Figure 3. Structure of the Reference Voltage

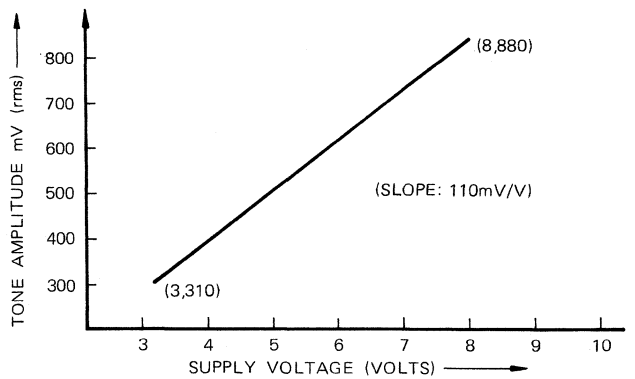
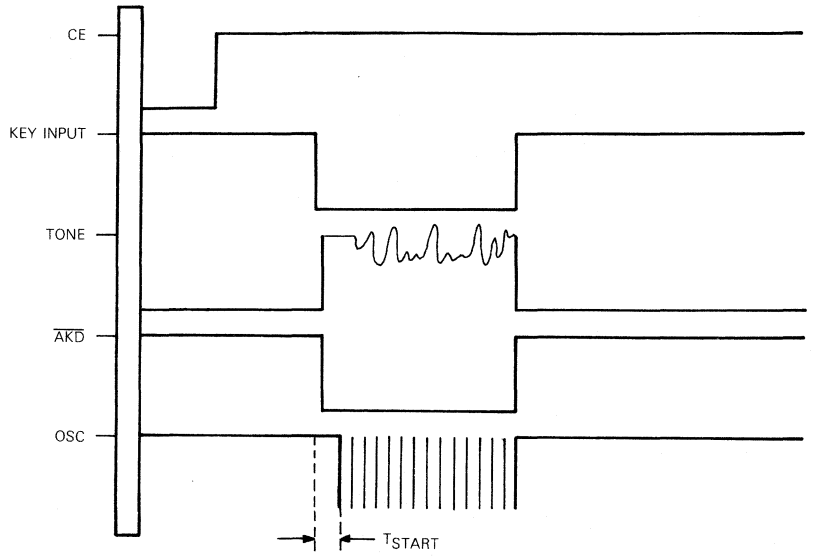
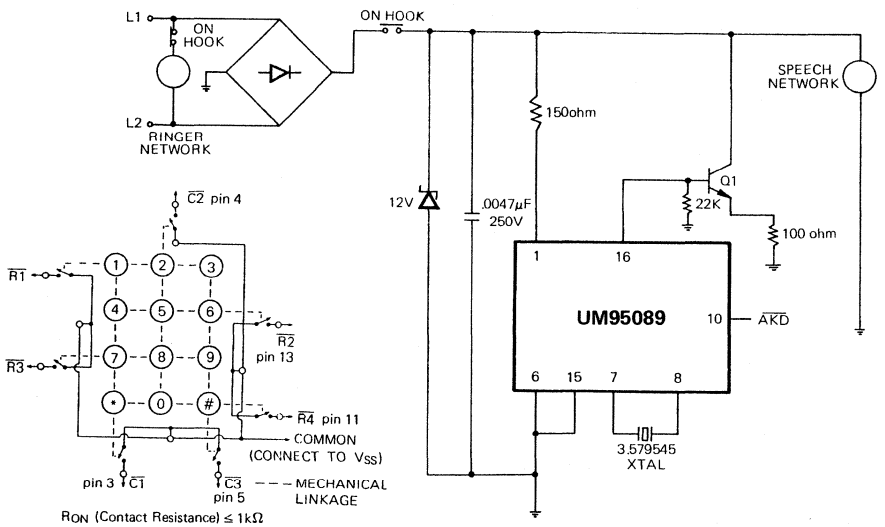


Figure 4. Typical Single Tone Output Amplitude VS. Supply Voltage (R_L = 10K)

Timing Diagram



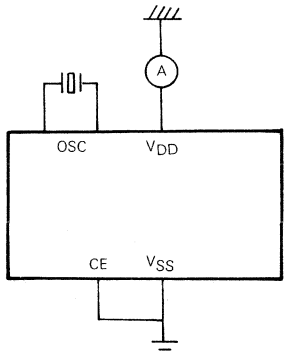
Application Circuit



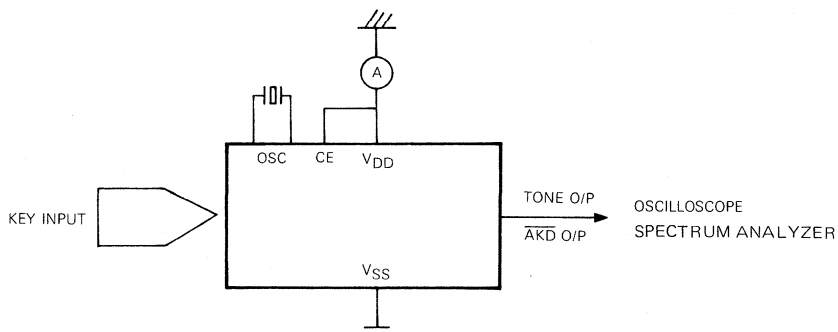
Standard Telephone Push Button Keyboard

Test Circuits

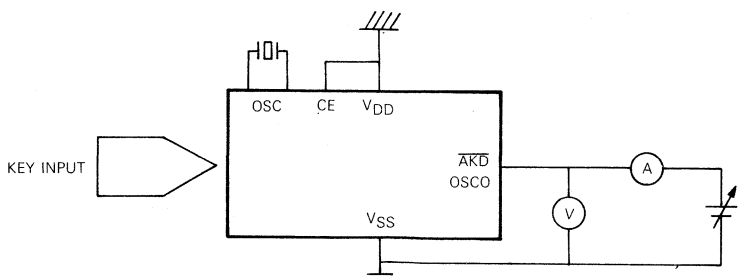
(A)



(B)



(C)



UMC

UM9559E/F

Tone Dialer

Features

- Low output tone distortion: 7%.
- Wide operating supply voltage range: 2.5 to 10.0 volts.
- TV crystal standard (3.58 MHz) used to derive all frequencies, providing high accuracy and stability.
- On-chip bias resistor for oscillator.
- Device power derived directly from telephone lines or from small batteries.
- On-chip mute drivers.
- On-chip reference voltage to assure amplitude stability.
- Direct interface to standard telephone keyboard or calculator-type XY keyboard.

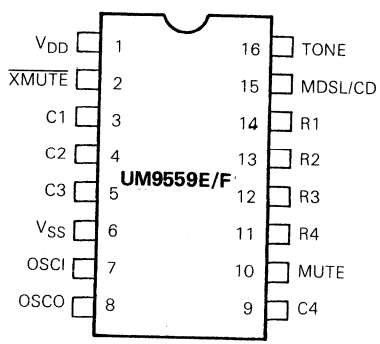
General Description

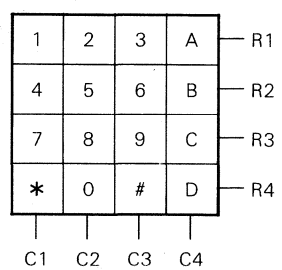
The UM9559E/F DTMF tone generator is designed to be used in a dual-tone telephone dialing system. The device may be connected directly to a standard push button telephone keyboard or calculator-type XY keyboard and operates directly from the telephone lines. The UM9559E/F derives all dual-tone frequencies from the widely used TV crystal standard, providing high accuracy and stability. The sinusoidal waveforms required for individual tones are digitally synthesized on the chip, resulting in waveforms with very low total harmonic distortion (7%). A stable reference voltage is also generated on the chip and is used to regulate the signal levels of the dual tones to ensure that they meet telephone industry specifications. With a slight modification of the standard 500 type basic telephone circuitry the UM9559E/F may be incorporated into a push button dual-tone telephone. Other applications of this device include radio and mobile telephones, remote control devices, and credit card verification terminals. The UM9559E/F is pin compatible with the S2559C/E and the S2559D/F, depending on which of two options for the function of pin 15 is selected.

Ordering Information

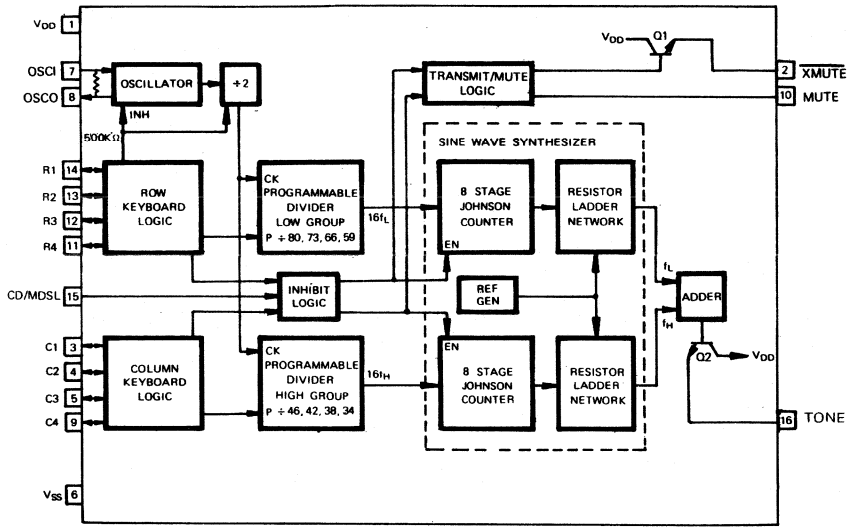
Part No.	Pin 15 Function
UM9559E	Mode Select
UM9559F	Chip Disable

Pin Configuration & Keyboard Assignments





Block Diagram



Absolute Maximum Ratings*

Power supply voltage (V_{DD} - V_{SS}) . . . . . -0.3V to +10.5V
Input voltage (V_{IN}) . . . . . -0.3V to V_{DD} + 0.3V
Maximum power dissipation (at 25°C) . . . . . 500 mW
Operating temperature (T_{OP}) . . . . . -20°C to +70°C
Storage temperature (T_{STG}) . . . . . -55°C to +150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(T_{OP} = 25°C, F_{OSC} = 3.579545 MHz)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD1}	2.5		10	V	Valid Key Input (tone output mode)	B
	V_{DD2}	2.0		10	V	No Key Input (Non-tone output mode)	
Supply Operating Current	I_{DD1}		1.0	2.0	mA	V_{DD} = 3.0V, one key input, all outputs unloaded	B
	I_{DD2}		8	16	mA	V_{DD} = 10.0V, one key input, all outputs unloaded	
Standby Current	I_{SD1}		0.3	30	μA	V_{DD} = 3.0V, no key input, all outputs unloaded	A
	I_{SD2}		1.0	100	μA	V_{DD} = 10.0V, no key input, all outputs unloaded	C
Mute Output Drive Current	I_{OH1}	0.17	0.41		mA	V_{DD} = 3.0V, V_{OH} = 2.5V	C
	I_{OH2}	0.57	1.5		mA	V_{DD} = 10.0V, V_{OH} = 9.5V	
Mute Output Sink Current	I_{OL1}	0.53	1.3		mA	V_{DD} = 3.0V, V_{OL} = 0.5V	C
	I_{OL2}	2.3	5.3		mA	V_{DD} = 10.0V, V_{OL} = 0.5V	
$\overline{\text{XMUTE}}$ Output voltage	V_{OH1}	0.8	1		VDD	V_{DD} = 3.0V, I_{OH} = 15 mA, no key input	C
	V_{OH2}	0.8	1		V_{DD}	V_{DD} = 10.0V, I_{OH} = 50 mA, no key input	
$\overline{\text{XMUTE}}$ Output Drive Leakage Current	I_{OF}			100	μA	V_{DD} = 10.0V, V_{OF} = 0.V	C

DC Characteristics (Continued)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Mute Output Voltage High	V_{OH1}	2.5	2.75		V	V_{DD} = 2.75V, one key input, no load	C
	V_{OH2}	9.5	10		V	V_{DD} = 10.0V, one key input, no load	
Mute Output Voltage Low	V_{OL1}		0.	0.5	V	V_{DD} = 2.75V, no key input, no load	C
	V_{OL2}		0.	0.5	V	V_{DD} = 10.0V, no key input, no load	
Mode Select Input Drive Current (UM9559E)	I_{IH1}	1.0	3.0		μA	V_{DD} = 3.0V, V_{IH} = 0.V (pull-up)	C
	I_{IH2}	1.3	2.0		μA	V_{DD} = 10.0V, V_{IH} = 3.0V (pull-up)	
Chip Disable Input Sink Current (UM9559F)	I_{IL1}	3.0	8		μA	V_{DD} = 3.0V, V_{IL} = 3.0V (pull-down)	
	I_{IL2}	25	37		μA	V_{DD} = 10.0V, V_{IL} = 10.0V, (pull-down)	
Input Voltage Range	V_{IH}		0.	0.2	V_{DD}		
	V_{IL}		0.	0.2	V_{DD}		
Row & Column Input Drive Current	I_{IH1}		210		μA	V_{DD} = 3.0V, V_{IH} = 2.5V (pull-up)	D
	I_{IH2}		740		μA	V_{DD} = 10.0V, V_{IH} = 9.5V, (pull-up)	
Row & Column Input Sink Current	I_{IL1}		16		μA	V_{DD} = 3.0V, V_{IH} = 3.0V (pull-down)	D
	I_{IL2}		24		μA	V_{DD} = 10.0V, V_{IH} = 10.0V (pull-down)	
Single Row Tone Output Amplitude	V_{OR1}		1.38		Vp-p	V_{DD} = 3.5V, R_L = 390Ω	B
	V_{OR2}		1.60		Vp-p	V_{DD} = 5.0V, R_L = 390Ω	
	V_{OR3}		1.6		Vp-p	V_{DD} = 10.0V, R_L = 240Ω	
Single Column Tone Output Amplitude	V_{OC1}		1.64		Vp-p	V_{DD} = 3.5V, R_L = 390Ω	B
	V_{OC2}		1.9		Vp-p	V_{DD} = 5.0V, R_L = 390Ω	
	V_{OC3}		1.95		Vp-p	V_{DD} = 10.0V, R_L = 240Ω	
Pre-emphasis	T_{WIST}	1	2	3	dB	V_{DD} = 3.5 ~ 10.0V	B
Distortion*	DIS%			10	%	V_{DD} = 5V * NOTE	B
Oscillator Output Sink Current	I_{OL1}	0.21	0.52		mA	V_{DD} = 3.0V, V_{OL} = 0.5V, one key input	C
	I_{OL2}	0.8	2.1		mA	V_{DD} = 10.0V, V_{OL} = 0.5V, one key input	
Oscillator Output Drive Current	I_{OH1}	0.13	0.31		mA	V_{DD} = 3.0V, V_{OL} = 2.5V, no key input	C
	I_{OH2}	0.42	1.1		mA	V_{DD} = 10.0V, V_{OL} = 9.5V, no key input	
Input/Output Capacitance	C_{IO1}	12	16		pF	V_{DD} = 3.5V	
	C_{IO2}	10	14		pF	V_{DD} = 10.0V	

*** Note:**

$$DIS\ (\%) = \frac{100 \times (V_1^2 + V_2^2 + \ldots + Vn^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$$

1. $V_1 \ldots Vn$ are the intermodulation and harmonic frequencies in the 500 to 3400 Hz band, and
2. VIl, VIH are the individual frequency components of the DTMF signal.

AC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator Start-up time	T_{START1}	V_{DD} = 3.5V		30		ms
	T_{START2}	V_{DD} = 10.0V		15		ms

R/C	Conditions	Spec.	Actual	Error (%)	Unit
R1	Fosc = 3.579545 MHz	697	699.1	+0.30	Hz
R2		770	766.2	-0.49	Hz
R3		852	847.4	-0.54	Hz
R4		941	948.0	+0.74	Hz
C1		1209	1215.9	+0.57	Hz
C2		1336	1331.7	-0.32	Hz
C3		1477	1471.9	-0.35	Hz
C4		1633	1645.0	+0.73	Hz

Note: % error does not include oscillator drift.

Pin Description

Pin	Designation	Description
1 6	V_{DD} V_{SS}	Positive and negative power supply inputs. The UM9559E/F is designed to operate from 2.5 to 10 volts.
2	$\overline{\text{XMUTE}}$	$\overline{\text{XMUTE}}$ output. This output is a bipolar NPN transistor. When no keys are depressed or the Chip Disable input is high (see description of pin 15), the $\overline{\text{XMUTE}}$ output is in the active state, allowing substantial current to be sourced to a load. When a key is depressed, the $\overline{\text{XMUTE}}$ output changes to a high impedance state.
3 4 5 9 11 12 13 14	C1 ~ C4 R4 ~ R1	Keyboard inputs An active pull-down on the row inputs and pull-up on the column inputs is present when no keys are depressed. When a key is depressed , a high will appear on one of the row inputs; this will cause the oscillator to start up and the keyboard scan logic to begin operating. The active pull-up and pull-down resistors will be switched on and off automatically as the keyboard scan logic determines the row and column pins that are selected. The advantage of the scanning technique is that an SPST keyboard arrangement (4 rows × 3 or 4 columns) can be used, and direct interface with CMOS logic outputs is possible. The UM9559E/F requires active high logic levels. Since the active pull-up resistors in the UM9559E/F are low valued (500Ω type), a diode can be used to eliminate excess sink current flow into the logic outputs during their low state.
7 8	OSCI OSCO	Oscillator Input/Output. The UM9559E/F contains a built-in oscillator circuit with two capacitors and a bias resistor, making it necessary to connect only a standard 3.58 MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator will be activated whenever a row input goes to high.

Pin Description (Continued)

Pin	Designation	Description
10	MUTE	Mute output. The UM9559E/F MUTE output is a CMOS buffer. When no keys are depressed or the Chip Disable input is high, the MUTE output is low. When a key is depressed the MUTE output is pulled high.
15	MDSL/CD	UM9559E: Mode select input. UM9559F: Chip disable input. The function of this pin is different in the E and F versions of the UM9559. In the UM9559E, this pin is the Mode Select input, while in the UM9559F it functions as a Chip Disable input. These two inputs are explained as follows: UM9559E MDSL: When MDSL is left floating or connected to V_{DD}, both dual and single-tone modes are available. When MDSL is connected to V_{SS}, single-tone mode is disabled and no output tone will be produced if an attempt to produce a single-tone output is made. In dual-tone mode a dual-tone output consisting of an appropriate high group and low group tone is generated whenever one row and column are selected (i.e. one key is depressed). If two digit keys that are neither in the same row nor column are depressed, dual-tone mode will be disabled and no output will be provided. In single tone mode, low group tones are generated by depressing two digit keys in the appropriate row. High group tones are generated by depressing two keys in the appropriate column. UM9559F CD: When the Chip Disable (CD) input is active high, tone output falls to VSS, all row and column inputs are at high impedance, the oscillator is inhibited, and the MUTE and $\overline{\text{XMUTE}}$ outputs are activated.
16	TONE	DTMF signal output The UM9559E/F uses Johnson counters and resistor ladder networks to synthesize the two desired frequencies in sine waves (see block diagram). An adder network is used to combine the two frequencies and then drive a bipolar NPN transistor connected as an emitter follower, thus allowing proper impedance transformation while preserving signal level.

Crystal Specification

Standard TV color burst crystals have a much tighter tolerance specification than is necessary for tone generation applications. Crystals with the following specifications are suggested for use with the UM9559E/F:

Frequency: 3.58 MHz ±0.02%
R_S = 100Ω, L_M = 96 mH, C_M = 0.02pF, C_H = 5pF, C_L = 12pF

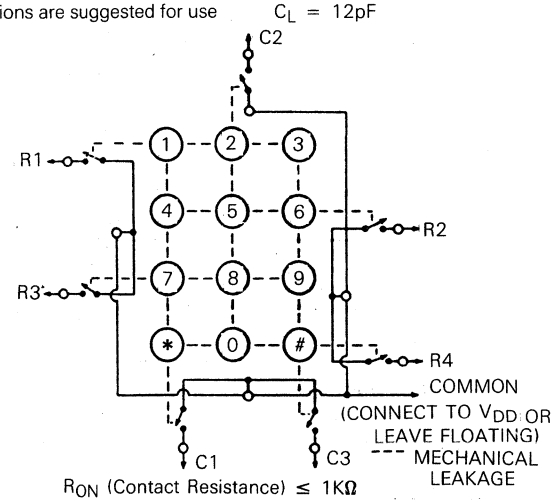


Figure 1: Standard Telephone Push button Keyboard

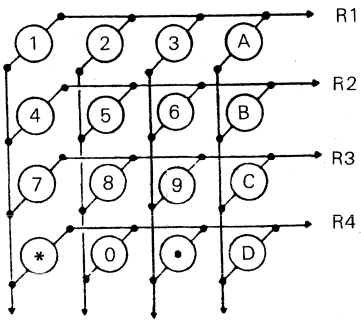


Figure 2 SPST Matrix Keyboard Arranged in the 2 of 8 Row Column Format

$\overline{\text{XMUTE}}$ and MUTE Functional Relationship

Output	'Digit' Key Released	'Digit' Key Depressed	Comment
$\overline{\text{XMUTE}}$	V_{DD}	High Impedance	Can drive at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can drive or sink current

DTMF Generator

The UM9559E/F has a well-designed digitally synthesized sine wave with a 15-level, 32-segment output structure.

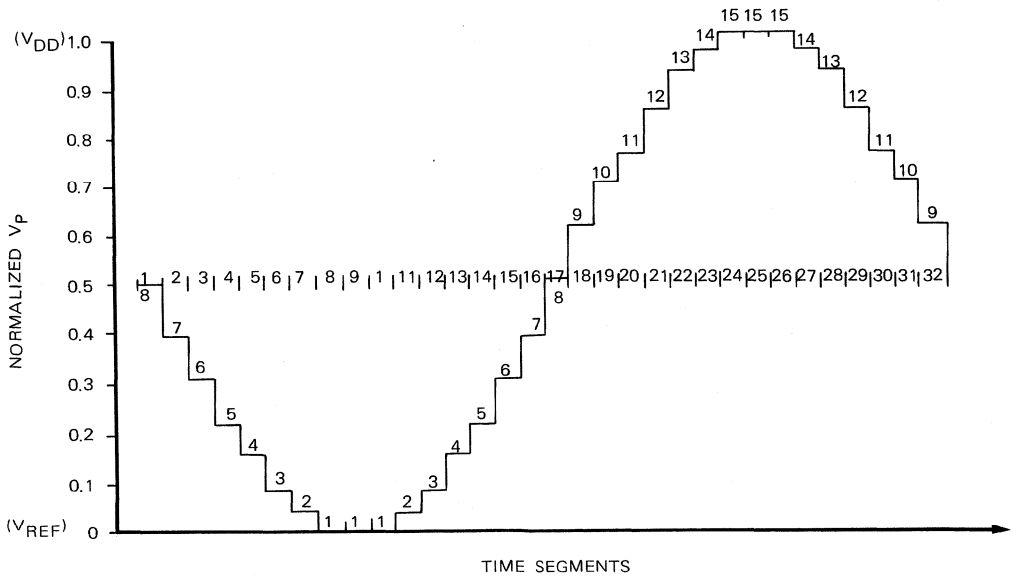
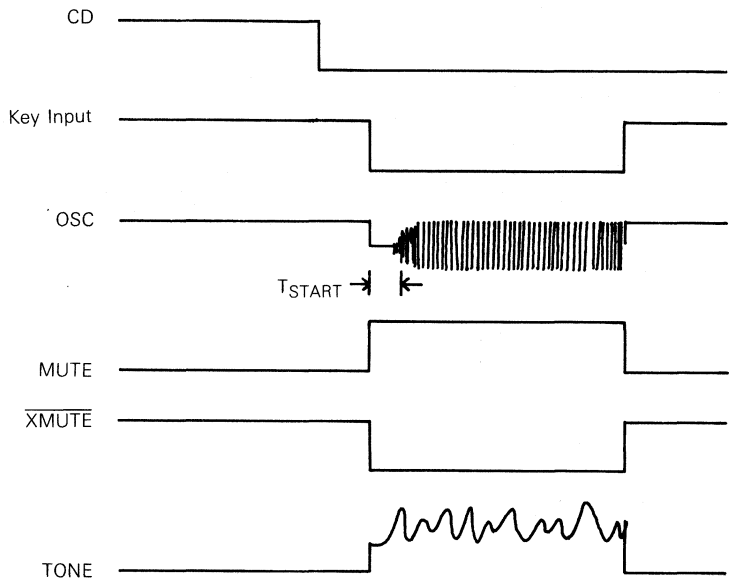


Figure 3. Single Tone Output Waveform

Timing Diagram



Application Circuits

1.

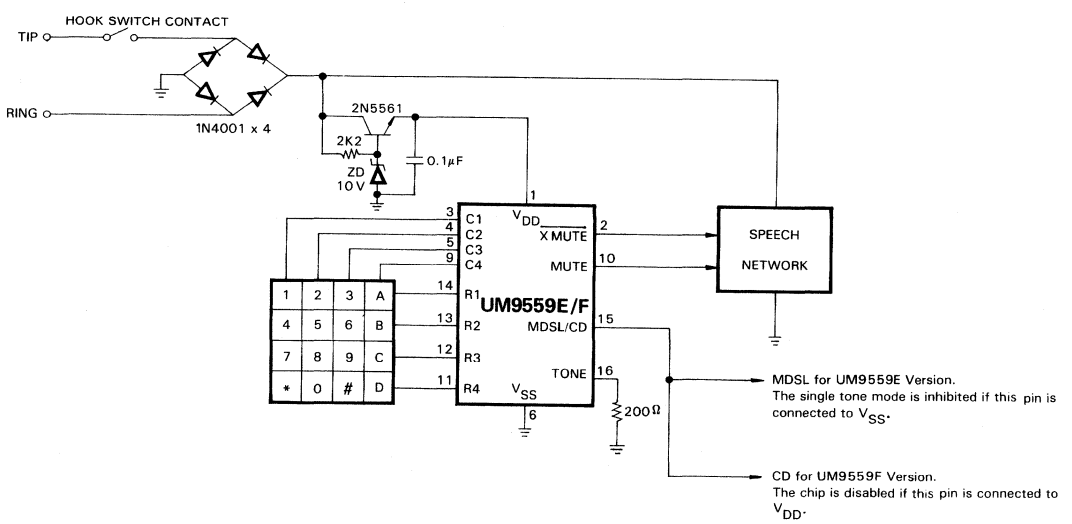
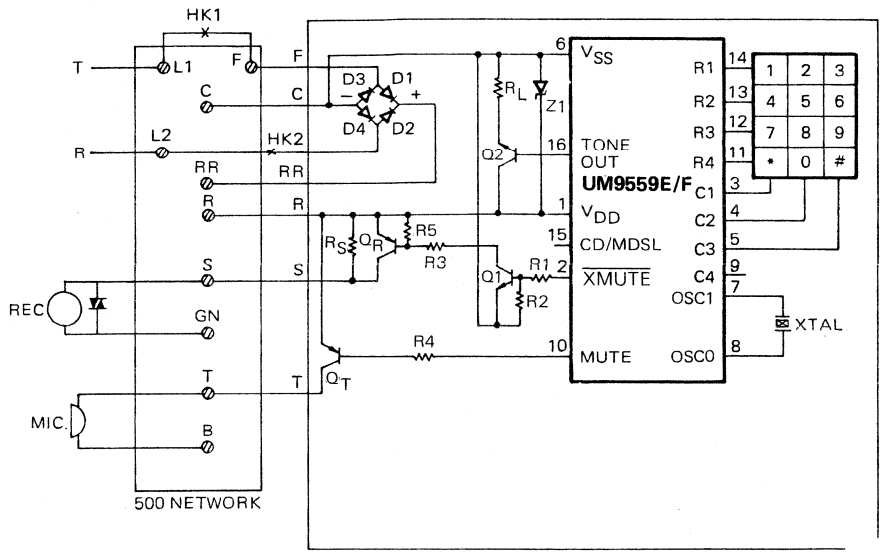


Figure 4 Tone Generator Interface Circuit

2.

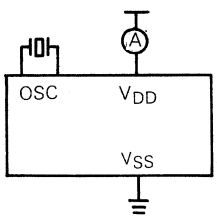


TYPICAL VALUES

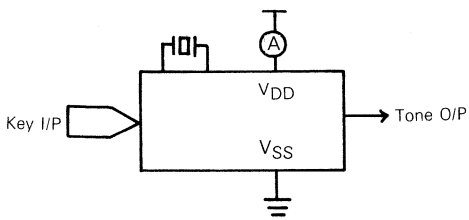
Z1:	1N4742 ZENER 12 VOLT	Q_R, Q_T:	2N4143
R_L:	150Ω, Q2: 2N4401, R_T: 10KΩ	D1-D4:	1N4004
Q1:	2N4401, R1: 10KΩ, R2: 30KΩ; R3: 2.7KΩ	XTAL:	3.58MHz
R4:	2.4KΩ, R5: 30KΩ, R_S: 5.1KΩ	C1:	.001μF

Test Circuits

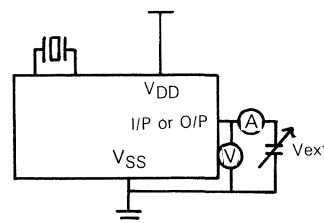
A)



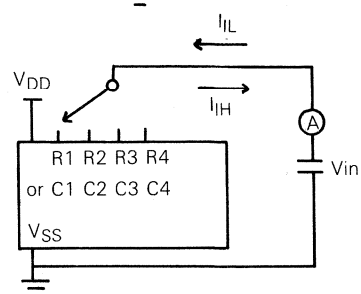
B)



C)



D)



Tone Dialer

Slave Dialer

Part No.	Description	Page
UM91531	Parallel Input Tone/Pulse Dialer	4-3

UMC

UM91531

Parallel Input Tone/Pulse Dialer

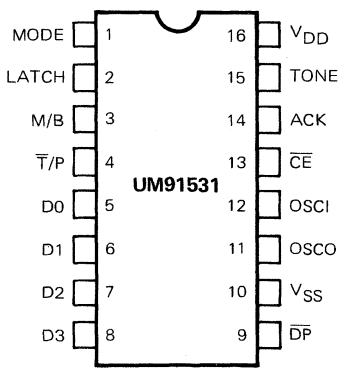
Features

- 4-bit parallel data input from microcomputer.
- TTL compatible inputs and outputs.
- Uses TV crystal standard (3.58 MHz) to derive all frequencies, providing high accuracy and stability.
- Operating voltage: 2.5 to 5.5 Volts.
- Selectable M/B ratio.
- 10 PPS dial rate.
- DTMF signaling of digits 0 — 9, *, #, A, B, C, and D.
- Pulse signaling of 0~9, *, #, and A.
- High group tone pre-emphasis: 2 dB.
- Low total harmonic distortion in DTMF signaling.
- RS-470 and CEPT compatible.

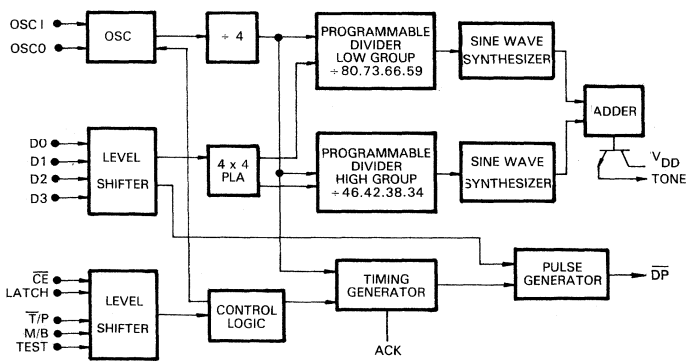
General Description

The UM91531 provides a 4-bit data input and a handshaking signal to serve as microcomputer interfaces. Under microcomputer control the UM91531 generates both a DTMF signal and a pulse output for telephone dialing. All necessary dual-tone frequencies and dial pulse outputs are derived from the widely used TV crystal standard, providing high accuracy and stability. The required sinusoidal waveform for individual tones is digitally synthesized on the chip, resulting in a waveform with very low total harmonic distortion.

Pin Configuration



Block Diagram



Slave Dialer

Absolute Maximum Ratings *

Power supply voltage (V_{DD}-V_{SS})..... −0.3V to +5.5V
Input voltage (V_{IN})..... −0.3V to V_{DD} + 0.3V
Maximum power dissipation (at 25°C).....600 mW
Operating temperature (T_{OP})..... −20°C to +60°C
Storage temperature (T_{STG})..... −55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0V, F_{OSC} = 3.579545 MHz, and T_{OP} = 25°C unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Operating Voltage	V_{DD}	2.5		5.5	V		B
Supply Operating Current	I_{DDP}		0.42	1	mA	$\overline{CE}=V_{SS}$	B
	I_{DDT}		0.42	1		All outputs unloaded	
Stand-by Current	I_{SD}		5	8	μA	$\overline{CE}=V_{DD}$ All outputs unloaded	A
$\overline{DP}$ Output Sink Current	I_{OL1}	1			mA	$V_{DD}=2.5V, V_{OL}=0.4V$	C
	I_{OL2}	3			mA	$V_{DD}=5.0V, V_{OL}=0.4V$	
Input Voltage Range	V_{IH}	0.8		1	V_{DD}		—
	V_{IL}	0		0.2			
Input Current Range	I_{IH}		0.05		μA		—
	I_{IL}		−0.05		μA		
Mode Pull-up Resistance	R_M	40			Kohm	$V_{DD}=2.5V$	—
		20			Kohm	$V_{DD}=5V$	C
ACK Source Current	I_{OHACK}	1.6			mA	$V_{DD}=5V, V_{OH}=2.4V$	C
ACK Sink Current	I_{OLACK}	4.0			mA	$V_{DD}=5V, V_{OL}=0.4V$	
D0,D1,D2,D3, T/P, M/B, LATCH, $\overline{CE}$	These pins TTL compatible I/O						—
Single Column Tone Output Amplitude	V_{OC}	770	840	910	mVp-p	$V_{DD}=2.5V$, $R_L=2.2Kohm$	B
		980	1070	1160		$V_{DD}=2.5V$, $R_L=2.2Kohm$	
Single Row Tone Output Amplitude	V_{OR}	980	1060	1160	mVp-p	$V_{DD}=5.5V$, $R_L=2.2Kohm$	B
		1250	1350	1450		$V_{DD}=2.5V$, $R_L=2.2Kohm$	
Pre-emphasis	Twist	1	2	3	dB		B
Valley of Single Tone	V_V		0.35		V_{DD}	$V_{DD}=3.5V$	B
Distortion	DIS		1	5	%	See note	B

Note: DIS (%) = $\dfrac{100(V_1^2 + V_2^2 + \ldots + Vn^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$

1) V_1....Vn are the intermodulations or harmonic frequencies in the 500 Hz to 3400 Hz band,
2) V_{IH}, V_{IL} are the individual frequency components of the DTMF signal.

AC Characteristics

(V_{DD} = 3.5V, V_{SS} = 0.V, F_{OSC} = 3.579545 MHz, T_{OP} = 25°C unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
PULSE						
Make/Break Ratio	M/B		1/2			M/B = V_{DD}
			2/3			M/B = V_{SS}
Make Time	T_M		33.3		ms	M/B = 1/2
			40			M/B = 2/3
Break Time	T_B		66.6		ms	M/B = 1/2
			60			M/B = 2/3
Inter-digit Pause Time	T_{IDP}		790		ms	M/B = 1/2
			783			M/B = 2/3
Predigit Pause	T_{PDP}		15		ms	M/B = 1/2
			15			M/B = 2/3
TONE						
Minimum Tone Duration	T_{MFD}		70		ms	
Minimum Tone Inter-digit Pause	T_{TIDP}		70		ms	
Tone Output Pre-digit Pause	T_{TPDP}		0		ms	
Oscillator Set-up Time	T_{START}		5		ms	

Row/Column	Condition	Spec.	Actual	Error (%)	Unit
R1	F_{OSC} = 3.579 MHz	697	699.1	+0.31	Hz
R2		770	766.2	−0.49	Hz
R3		852	847.4	−0.54	Hz
R4		941	948.0	+0.74	Hz
C1		1209	1215.9	+0.57	Hz
C2		1336	1331.7	−0.32	Hz
C3		1477	1471.9	−0.35	Hz
C4		1633	1645.0	+0.73	Hz

Note: % Error does not include oscillator drift.

Pin Description

Pin	Designation	Description
1	MODE	Tone mode select input. When this input is high, the tone output and ACK output are normal. When this input is low, a DTMF signal will be generated continuously and any new input data will be ignored. This input affects the tone output mode only.
2	LATCH	Latch input. When input on this pin changes from low to high (at the rising edge), the UM91531 latches the 4-bit input data and T/P input. The latch input should not be changed back from low to high again until the ACK output falls low, and new data must not be latched while the ACK output is still low.
3	M/B	Make/Break ratio select input. This pin is used to select one of two available make/break ratios. A high input selects the 2/3 make/break ratio; a low input selects the 1/2 ratio. This input should be connected to V_{DD} or V_{SS} only. Changing the state of this pin when $\overline{CE}$ is active (low) enables the test mode.
4	$\overline{T}$/P	Tone/pulse mode select input. This input determines whether tone or pulse mode will be activated. It is latched together with the 4-bit data input.
5—8	D0—D3	4-bit data input pins. This 4-bit parallel input is used to receive data generated by the microcomputer. (Input data vs. output signal is shown in table 1.) Valid input data should be presented at these inputs before and during the rising edge of the latch signal.
9	$\overline{DP}$	Dial pulse output. The dial pulse output consists of an N-channel open drain device. During dial pulse break periods this output is switched on (sinking current to V_{SS}); it is switched off during all other states. Dialing rate is 9.71 PPS and post-digit pause is 823 ms. (The output of this pin during test mode is discussed below.)
10 16	V_{SS} V_{DD}	Negative power supply input. Positive power supply input (operating range 2.5 to 5.5 volts).
11 12	OSCO OSCI	Oscillator output. Oscillator input. The UM91531 contains an oscillator circuit with the necessary parasitic capacitance and feedback resistor on chip, making it necessary to connect only a standard 3.58 MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. An external clock input can be applied to the OSCI pin directly. The oscillator is enabled when the $\overline{CE}$ input is low.
13	$\overline{CE}$	Chip enable input. This input controls the onset of oscillation and serves as the master reset for this device.
14	ACK	Acknowledge output. This pin provides an acknowledge signal to the microcomputer. This output is high when the device is ready to dial out the next digit; it falls low immediately after the rising edge of the latch signal.
15	TONE	DTMF signal output. This pin consists of an NPN transistor output, with the collector connected to V_{DD}. This pin is also connected to the emitter output. The internally generated DTMF signal is delivered to the base of the NPN transistor and is amplified as the transistor connected in common collector or darlington output forms. DTMF signaling output time is 70 ms and the interdigit interval is 70 ms. Typical output impedance of the DTMF signal is 1.25 Kohm, and the h_{FE} of the NPN transistor is at least 30 at I_C = 3 mA.

Functional Description

Input Data vs. Output Signal

Parallel binary signals on Do — D3 pins are input from microcomputer. Output signal vs. input data is shown in table 1:

D3	D2	D1	D0	DTMF Signaling	PULSE Signal (O/P Pulse No.)
0	0	0	0	0	10
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	*	10
1	0	1	1	#	11
1	1	0	0	A	12
1	1	0	1	B	13
1	1	1	0	C	14
1	1	1	1	D	Forbidden input

Table 1.

Input Data vs. Output Signal in Test Mode

The UM91531 provides a high speed pulse/tone output for testing consideration. If the M/B input changes state after the UM91531 is enabled, the test mode is initiated and the device will remain in test mode unless disabled. Table 2 shows input data vs. output signal in pulse/tone test mode.

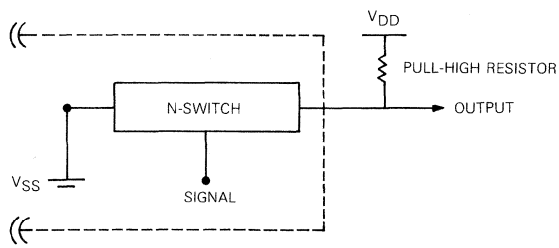
D3, D2, D1, D0 Input In Hex Code	Tone O/P Frequencies and Test Mode		Pulse O/P Frequencies and Test Mode
	Tone Pin O/P	$\overline{DP}$ Pin O/P	$\overline{DP}$ Pin O/P
0	948.0	1,331.7 x 8	10 x 48
1	699.1	1,215.9 x 8	1 x 48
2	1,331.7	699.1 x 8	2 x 48
3	1,417.9	699.1 x 8	3 x 48
4	1,215.9	766.2 x 8	4 x 48
5	1,331.7	766.2 x 8	5 x 48
6	766.2	1,471.9 x 8	6 x 48

D3, D2, D1, D0 Input In Hex Code	Tone O/P Frequencies and Test Mode		Pulse O/P Frequencies and Test Mode
	Tone Pin O/P	$\overline{DP}$ Pin O/P	$\overline{DP}$ Pin O/P
7	847.4	1,215.9 x 8	7 x 48
8	1,331.7	847.4 x 8	8 x 48
9	1,471.9	847.4 x 8	9 x 48
A	1,215.9	948.0 x 8	10 x 48
B	1,471.9	948.0 x 8	11 x 48
C	1,645.0	699.1 x 8	12 x 48
D	1,645.0	766.2 x 8	13 x 48
E	1,645.0	847.4 x 8	14 x 48
F	1,645.0	948.0 x 8	0

Note: Tone Pin O/P in sine wave, $\overline{DP}$ Pin O/P in square ware. The normal timing is reduced to 1/8 at tone test mode and 1/48 at pulse test mode.

Table 2.

N-Channel Open Drain Output



DTMF Generator

The DTMF signal is produced from the tone frequency generator circuit with an NPN transistor-emitter-follower output buffer (Figure 1). The digitally synthesized sinewave has a 7-level, 16 segment (1.1V + 1.3V) reference voltage (Figure 2). The DTMF's total harmonic distortion is 5% maximum. Total harmonic distortion (THD) vs. operating voltage and DTMF output vs. operating voltage is shown in Figures 3 and 4.

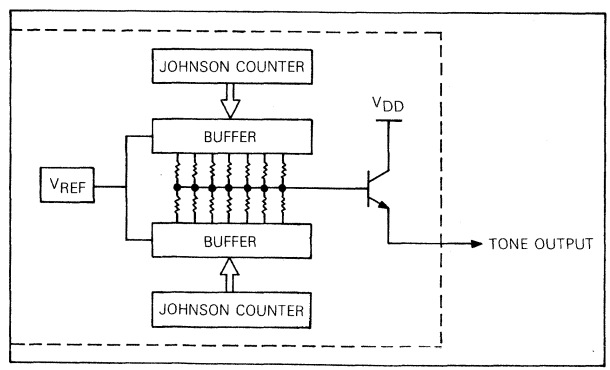


Figure 1

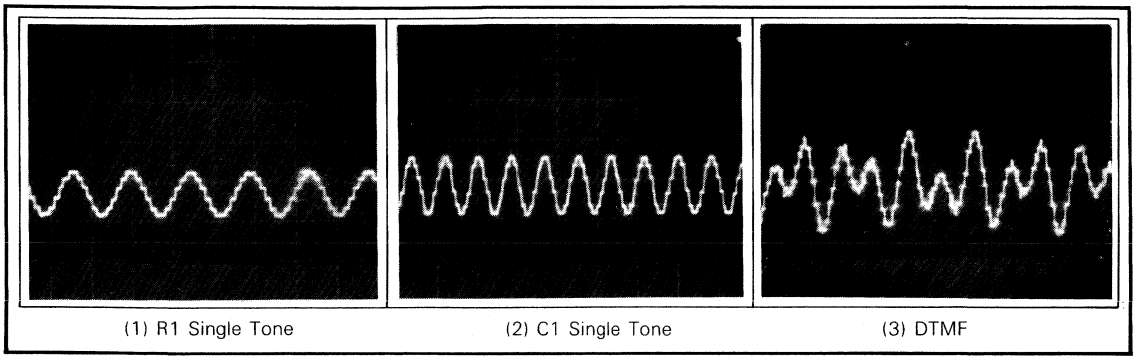
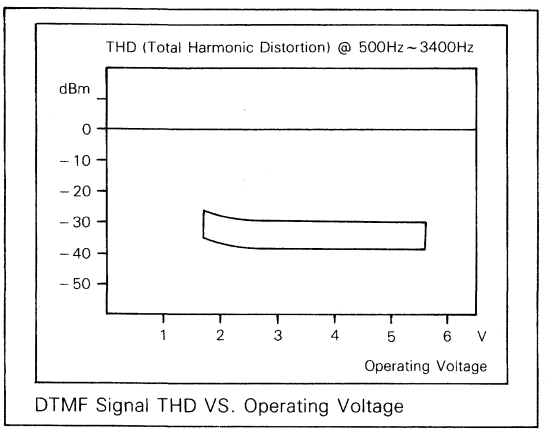
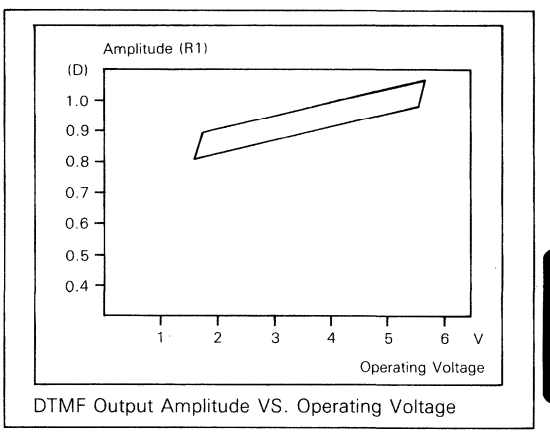


Figure 2. Waveforms



DTMF Signal THD VS. Operating Voltage

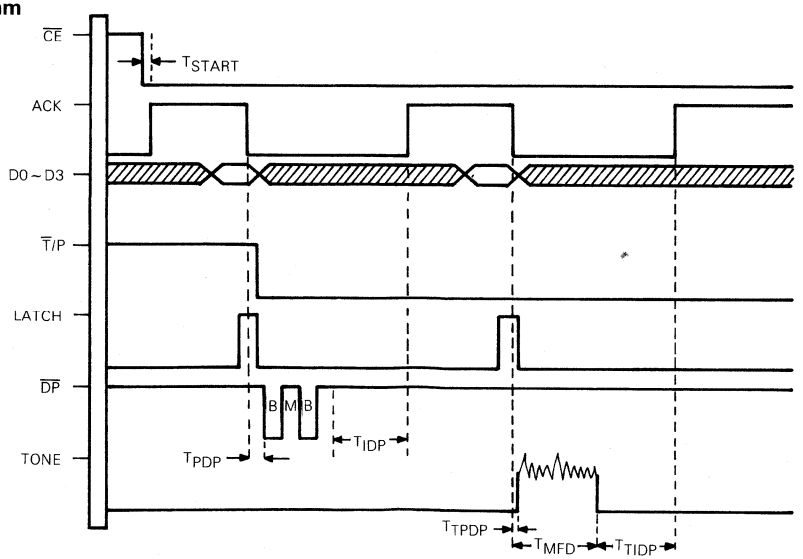
Figure 3.



DTMF Output Amplitude VS. Operating Voltage

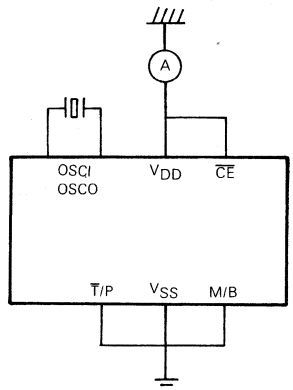
Figure 4.

Timing Diagram

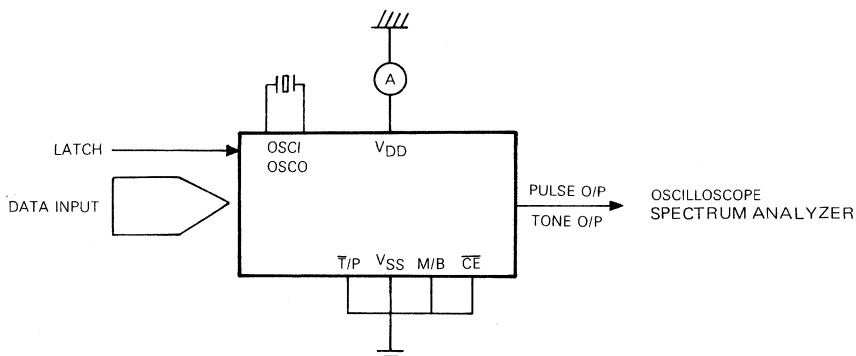


Test Circuits

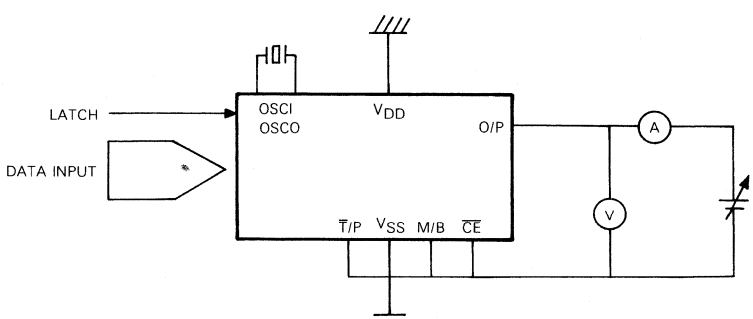
(A)



(B)



(C)



Telephone Related Products

Part No.	Description	Page
UM9203/04	DTMF Receiver	5-3
UM93510A/B/C	Speech Recording and Reproduction IC (with SRAM)	5-13
UM9310	Cordless Telephone Controller	5-24
UM93520A/B	Speech Recording and Reproduction IC (with DRAM)	5-38

UMC

UM9203/04

DTMF Receiver

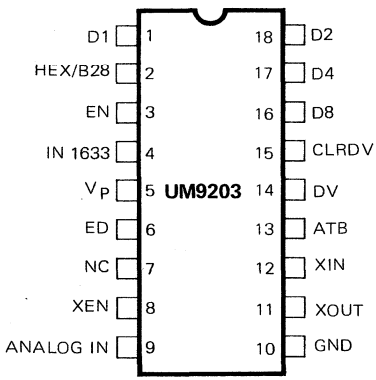
Features

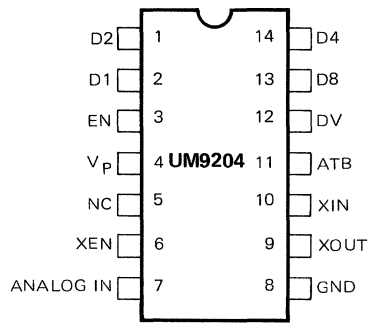
- Single 5-volt power supply.
- Detects either 12 (UM9203) or 16 (UM9203/04) standard DTMF digits.
- Output in either 4-bit hexadecimal code (UM9203/04) or 2-of-8 binary code (UM9203)
- Full DTMF receiver in a single 18-pin (UM9203) or 14-pin (UM9204) plastic DIP package.
- Tristate outputs.
- Early detect output (UM9203 only).
- Excellent speech immunity.

General Description

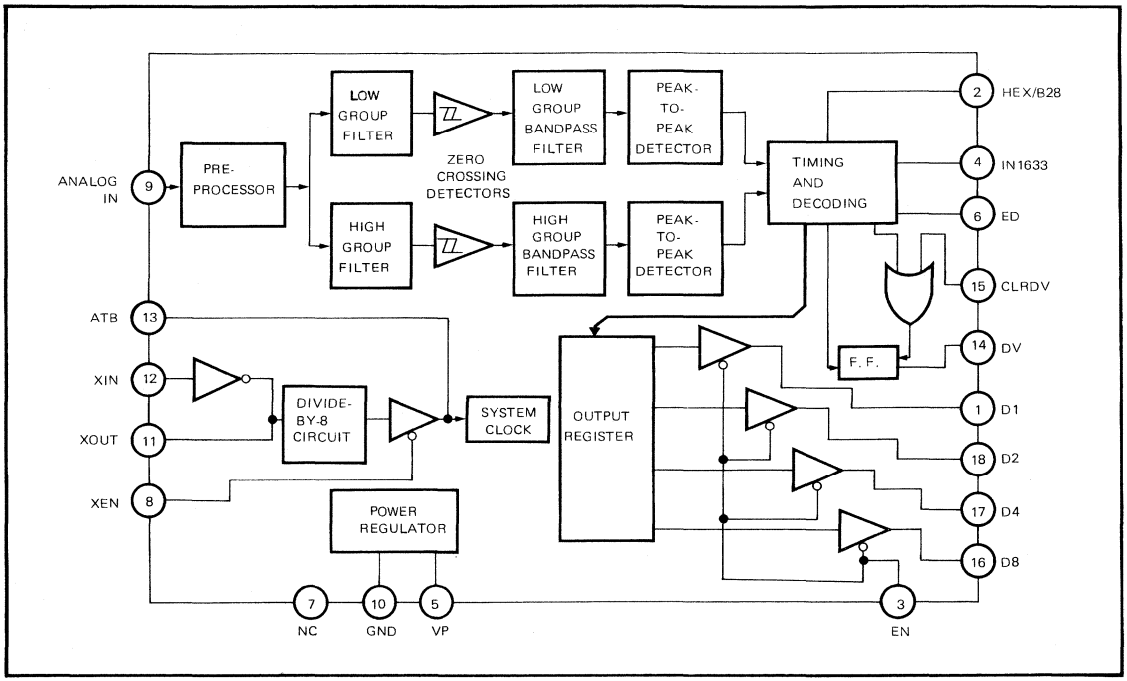
The UM9203/04 are single chip monolithic CMOS receivers designed to detect either 12 or 16 standard Dual Tone Multi-Frequency (DTMF) digits. The UM9203/04 includes a preprocessor, band split filters, zero crossing detectors, bandpass filters, peak-to-peak detectors and digital control circuits. No front-end pre-filtering is needed; the only external components required are a 3.579545 MHz crystal and a bias resistor. The UM9203/04 is packaged in a standard 18-pin (UM9203) or 14-pin (UM9204), plastic DIP and requires only a single voltage supply. The UM9203/04 provides tristate data outputs in either 4-bit hexadecimal code (UM9203/04) or 2-of-8 binary code (UM9203) and can be easily interfaced with a standard CMOS digital system.

Pin Configurations

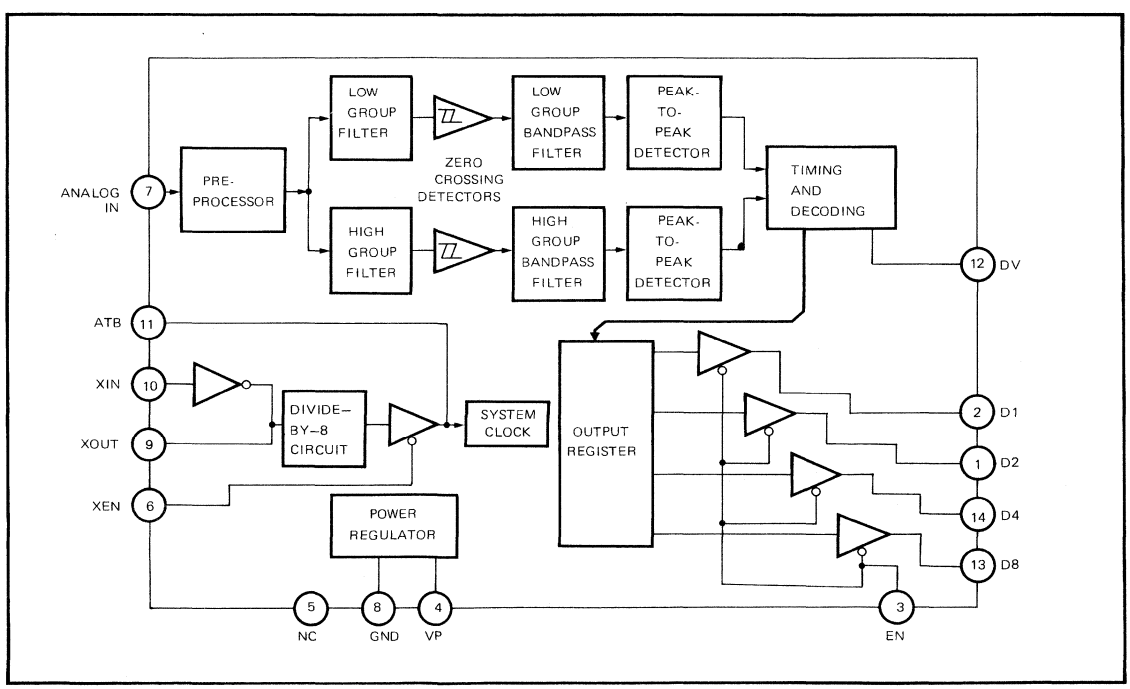




UM9203 Block Diagram



UM9204 Block Diagram



Pin Description

Pin		Symbol	Description
UM9203	UM9204		
1 18 17 16	2 1 14 13	D1 D2 D4 D8	Data outputs. These digital outputs provide codes (in UM9203 the code format can be programmed by the HEX/B28 pin) corresponding to detected digits. These outputs become valid after a tone pair has been detected and are cleared when a valid pause has been timed.
2	–	HEX/B28	Digital output format control. When this pin is pulled high, the UM9203's output is given in hexadecimal code. When input is low, output is in 2-of-8 binary code. Output codes are shown in Table 1.
3	3	EN	Output enable. When EN is pulled high, the data outputs are in the CMOS push-pull state and represent the contents of the register. When EN is low, the data outputs are forced to the high-impedance state.
4	–	IN1633	DTMF signal control. When this pin is pulled high, detection of tone pairs containing the 1633 Hz component is inhibited. To detect all 16 standard digits this pin must be pulled low.
5	4	V_P	Positive power supply connection.
6	–	ED	Early signal detection output. ED goes to high when the UM9203 begins to detect a DTMF tone pair and falls to low when a pause is detected. While the data outputs will definitely be valid when DV is high, they will not necessarily be valid when ED is high. Thus the ED output can be used to determine if signals are reaching the DTMF receiver.
7	5	NC	Not connected. This pin has no internal connection and may be left floating or connected to GND.
8	6	XEN	Crystal oscillator enable. Pulling XEN high will enable the crystal oscillator.
9	7	ANALOG IN	DTMF input. This pin is internally biased so that the input signal may be AC coupled. This input may also be DC coupled as long as voltage does not exceed that of the positive power supply. Proper input coupling is illustrated in Figure 1.
10	8	GND	Negative power supply connection.

Pin Description (Continued)

Pin		Symbol	Description
UM9203	UM9204		
12 11	10 9	XIN XOUT	Crystal connections. The XIN and XOUT pins are the input and output of an on-chip inverter. A complete oscillator circuit is formed by connecting a 3.579545 MHz color-burst crystal and a 1M resistor between XIN and XOUT.
13	11	ATB	Auxiliary time base In/Output. When XEN is pulled high, this pin can be used to provide a clock frequency time base for up to ten other UM9203/04s. When XIN is pulled high and XEN low, this pin acts as an auxiliary time base input. (Auxiliary input must equal 3.579545 MHz divided by 8 for the UM9203/04 to meet specifications.)
14	12	DV	Valid data indication output. DV goes high after a valid tone pair has been detected at Analog In and decoded at the data outputs. DV remains high until a valid pause is detected or the CLRDV input is raised high, whichever occurs first.
15	–	CLRDV	DV clear. When CLRDV is pulled high, DV is reset to the low state.

Digit	Hexadecimal				Binary Coded 2 of 8				Low Group Frequency (Hz)	High Group Frequency (Hz)
	D8	D4	D2	D1	D8	D4	D2	D1		
1	0	0	0	1	0	0	0	0	697	1209
2	0	0	1	0	0	0	0	1	697	1336
3	0	0	1	1	0	0	1	0	697	1477
4	0	1	0	0	0	1	0	0	770	1209
5	0	1	0	1	0	1	0	1	770	1336
6	0	1	1	0	0	1	1	0	770	1477
7	0	1	1	1	1	0	0	0	852	1209
8	1	0	0	0	1	0	0	1	852	1336
9	1	0	0	1	1	0	1	0	852	1477
0	1	0	1	0	1	1	0	1	941	1336
*	1	0	1	1	1	1	0	0	941	1209
#	1	1	0	0	1	1	1	0	941	1477
A	1	1	0	1	0	0	1	1	697	1633
B	1	1	1	0	0	1	1	1	770	1633
C	1	1	1	1	1	0	1	1	852	1633
D	0	0	0	0	1	1	1	1	941	1633

Table 1. DTMF Signal Output Codes

Functional Description

The general operation of the UM9203/04 is described as follows:

Preprocessor

A 60 Hz reject filter and a pre-emphasis amplifier are included in the preprocessor. An input protection circuit has been placed in front of the preprocessor to prevent the chip input from damage due to high voltage. The function of the preprocessor is to emphasize the high frequency components of the input signal in order to compensate for signal loss due to transmission through the telephone lines.

Band Split Filters

The band split filters consist of two high order band rejection filters. The output signals of the band split filters are split into high and low frequency groups. The separated tones are then put through gain stages and sent to the zero-crossing detectors.

Zero-Crossing Detectors

Signals emerging from the band-split filters are converted into square waves in the zero-crossing detectors. The square waves are then sent through four bandpass filters each for both the high and low frequency groups. If the original DTMF input signals are not pure tones, then the converted square wave outputs will have variable periods.

Bandpass Filters

The eight bandpass filters are divided into two groups, corresponding to the high and low frequency groups, and are used to detect input signals corresponding to one of the eight different standard frequencies used in DTMF signaling systems. When an input signal falls inside one of these frequency bands, the corresponding bandpass filter will go to high, allowing it to be detected by the peak-to-peak detectors.

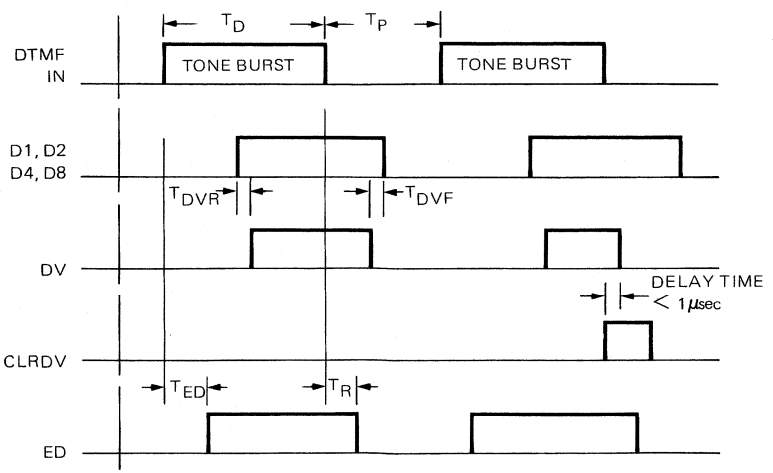
Peak-to-Peak Detectors

The output of each bandpass filter is monitored using the multiplex method. In each of the two tone groups, only one bandpass filter at a time will go to high and remain in the high state long enough to be considered valid; valid high-level outputs will then be detected by the peak-to-peak detectors.

Timing and Decoding

The outputs of the peak-to-peak detectors are decoded into either 4-bit hexadecimal code (UM9203/04) or 2-of-8 binary code (UM9203). The ED (Early Detection, UM9203) pin can be used to indicate the presence of a signal input; ED will go to high within 20 msec after a DTMF input is detected. Within 46 msec of reception of a DTMF signal the DV pin should go to high as well, indicating that valid data has been received. When an input signal is no longer present, ED and DV will both drop to low within 18 and 50 msec respectively. DV can also be reset to low by pulling CLRDV to high.

Timing Diagram



Absolute Maximum Ratings*

DC Supply Voltage (V_P) 7.0V
Analog In Voltage . . . . . $V_P - 10V$ to $V_P + 0.5V$
Input Voltage (any pin except Analog In)
. . . . . $-0.5V$ to $V_P + 0.5V$
DC Current Into Any Input . . . . -10.0 mA to $+10.0$ mA
Operating Temperature (T_{OP}) . . . . . 0°C to 70°C
Storage Temperature (T_{STG}) . . . . . -55°C to $+150$°C
Power Dissipation . . . . . 880 mW
Lead Temperature (soldering 10 sec) . . . . . 256°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

($V_P = 5.0V$, $V_{SS} = 0V$, $F_{OSC} = 3.579545$ MHz, $T_{OP} = 25$°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High-Level Input Voltage	V_{IH}	$0.7V_P$	–	V_P	V	
Low-Level Input Voltage	V_{IL}	0	–	$0.3V_P$	V	
High-Level Output Voltage (Except XOUT Pin)	V_{OH}	$V_P - 0.5$	–	V_P	V	200μA Load
Low-Level Output Voltage (Except XOUT Pin)	V_{OL}	0	–	0.5	V	400μA Load
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	
Supply Current	I_{DD}		10	16	mA	

AC Electrical Characteristics

($V_P = 5.0V$, $V_{SS} = 0V$, $F_{OSC} = 3.579545$ MHz, $T_{OP} = 25$°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Frequency Deviation Accept Limit				±1.5±2Hz	% of f_0	MITEL tape #7291 (See Note 1)	Fig. 8
Frequency Deviation Reject Limit		±3.5			% of f_0	MITEL tape #7291 (See Note 1)	Fig. 8
Amplitude for Detection		–32		–2	dBm	MITEL tape #7291	Fig. 8
Minimum Accept Twist		–10		10	dB	MITEL tape #7291	Fig. 8
Noise Tolerance				–12	dB	MITEL tape #7291	Fig. 8
60 Hz Tolerance				0.8	V_{rms}		
Power Supply Noise				10	mV_{P-P}		
Talk-off			4		hits	MITEL tape #7291	Fig. 8
Input Impedance	Z_{IN}		100KΩ //15pF				

Note 1: If dial tone frequency deviation is less than ±(1.5)% of f_0, the receiver will work very well. If dial tone frequency deviation is larger than ±(1.5)% and less than ±(3.5)% of f_0, it is possible to find errors on the data output. If dial tone frequency deviation is larger than ±(3.5)% of f_0, then the receiver will not work.

Switching Characteristics

(V_P = 5.0V, V_{SS} = 0V, F_{OSC} = 3.579545 MHz, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Ckt.
Tone Time for detect	T_{ON}	40	–	–	ms	MITEL tape #7291	Fig. 8
Tone Time for reject	T_{ON}	–	–	20	ms		
Pause Time for detect	T_{OFF}	40	–	–	ms	MITEL tape #7291	Fig. 8
Pause Time for reject	T_{OFF}	–	–	20	ms		
Detect Time	T_D	25	–	46	ms		
Release Time	T_R	25	–	50	ms		
Data Setup Time	T_{SU}	7	–	–	μs		
Data Hold Time	T_H	7	9	10	μs		
DV Clear Time	T_{CL}	–	160	250	ns		
CLRDV Pulse Width	T_{PW}	200	–	–	ns		
ED Detect Time	T_{ED}	7	–	20	ms		
ED Release Time	T_{ER}	2	–	18	ms		
Output Enable Time C_L = 50 pF, R_L = 1 KΩ	T_{EN}	–	200	300	ns		
Output Disable Time C_L = 35 pF, R_L = 500 Ω	T_{DIS}	–	150	200	ns		
Output Rise Time C_L = 50 pF	T_{RISE}	–	200	300	ns		
Output Fall Time C_L = 50 pF	T_{FALL}	–	160	250	ns		

Note: R_L and C_L are parallel impedances taken to GND

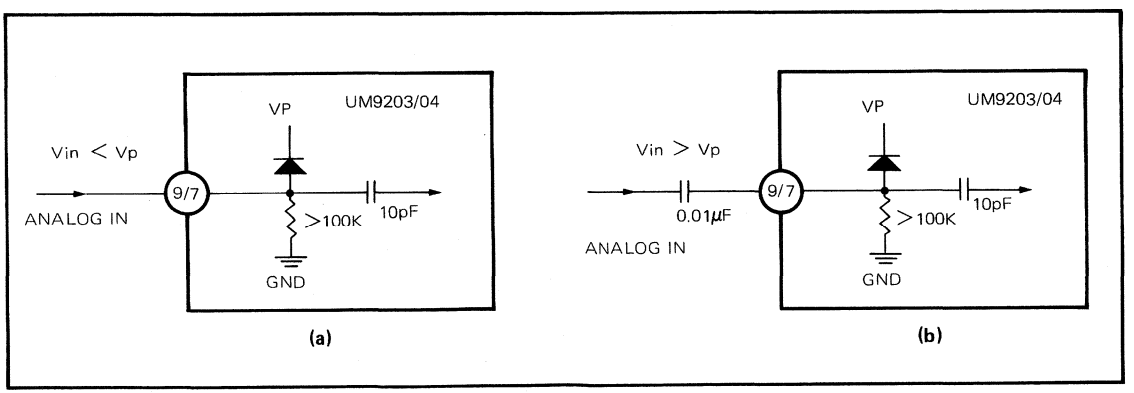


Figure 1. Input Signal Coupling

Applications

DTMF receivers have a variety of applications, including use in PBXs, toll call restrictors, answering machines with remote control, credit card verification and inquiry systems, and other automation and remote control systems. Due to their high noise immunity, DTMF signals constitute a communication method with a very low error rate, and are utilized as data carriers in a variety of communication systems.

Single-Chip DTMF signal generators and receivers greatly simplify the implementation of a DTMF communication system. A typical DTMF communication system application is shown in Figure 2. In addition, several application circuits are described below:

Telephone Line Input Interfaces

Three suggested types of input circuits for interfacing the UM9203/04 to telephone lines are illustrated in Figures 3, 4, and 5.

Input Circuit with Dial Tone Reject Filter

The dial tone reject filter shown in Figure 6 is an elliptic highpass filter. It is a second-order RC-active filter with two operational amplifiers. The filter is designed with cutoff frequency 460 Hz and provides a minimum of 18 dB rejection at 330 Hz and 440 Hz. Hence, this filter improves dial tone tolerance at least 18 dB for a DTMF decoding system, where dial tone tolerance is defined as the total power of precise dial tone (350 Hz and 440 Hz as equal amplitudes) relative to the lowest amplitude tone in a valid tone pair. The operational amplifiers could be UA741, LM1458 or equivalents. The component tolerance in the filter is 1% for resistors and 5% for capacitors.

Microcomputer or Microprocessor Interfaces

The UM9203 can be connected directly to a microprocessor or single-chip microcomputer such as the 8048 or 8051. In Figure 7a, the data outputs of the UM9203 are connected to the I/O ports of the microcontroller in such a way that the EN pin on the UM9203 will remain in a constant high state. In Figure 7b, the UM9203 data outputs share the same data bus as the microcontroller. Thus the UM9203 EN pin must be controlled by the microcontroller in order to differentiate DTMF data from other data sources that will be using the same data bus. In this case, when the output signal P27 of the microcontroller is pulled high, the microcontroller 8048 will read the UM9203 output data, when P27 is set to low, the microcontroller 8048 will read data from other sources. In order to prevent the microcontroller from being reset during the execution of an interrupt service routine, the UM9203 DV pin can be reset to low state by pulling CLRDV to high.

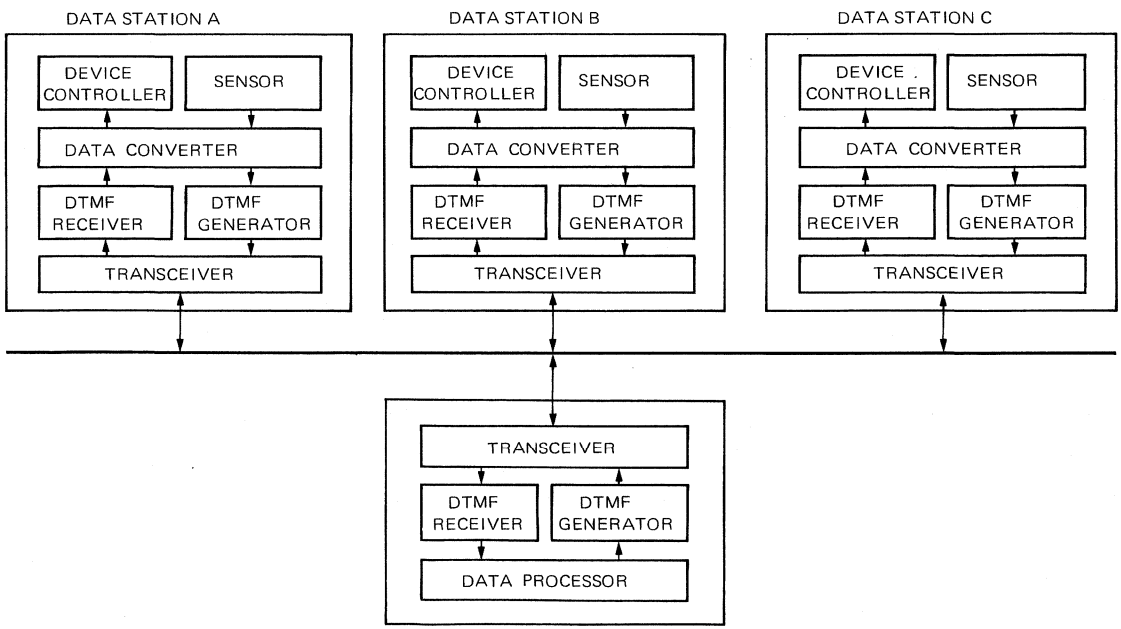


Figure 2. DTMF Data Communication System

Applications Circuits

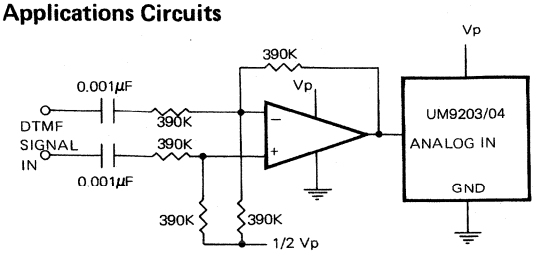


Figure 3. Line input circuit (A)

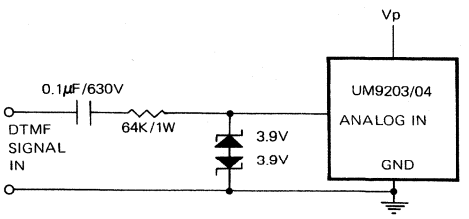


Figure 4. Line input circuit (B)

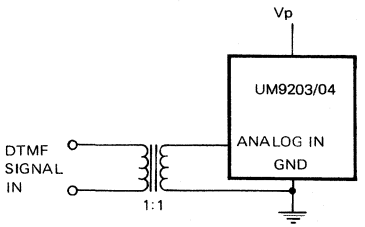


Figure 5. Line input circuit (C)

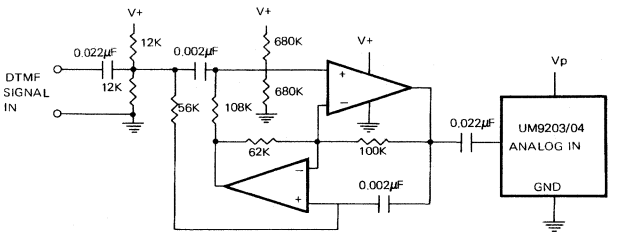


Figure 6. Dial tone reject filter

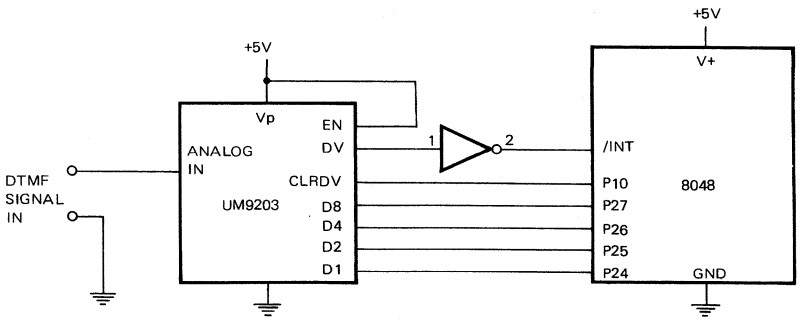


Figure 7(a). Interface with microprocessor

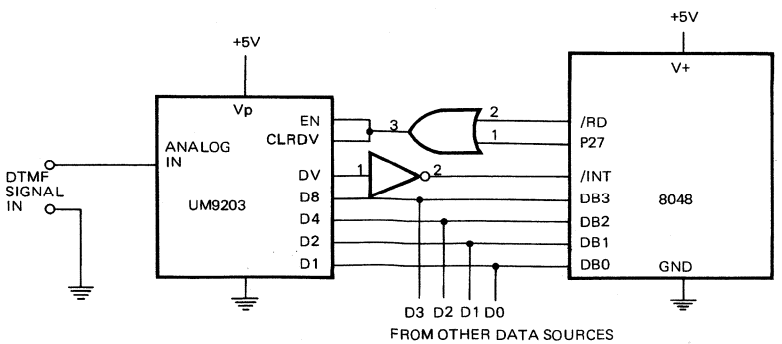


Figure 7(b). Interface with microprocessor

Test Circuit

The test circuit for the UM9203/04 is shown in Figure 8. The Mitel CM7291 Tone Receiver Cassette should be used to evaluate the UM9203/04. Other testing equipment should include a digital counter, an AC voltmeter, a cassette tape player, and a small amplifier for adjusting the level of the tone at the receiver input. The CM7291 tape contains a series of tests consisting of recorded tone bursts with the parameters varied in a number of ways. Tests are performed by sending the tone bursts to the receiver and counting the number of bursts to which the receiver responds. Results from these tests provide a direct indication of the receiver's performance.

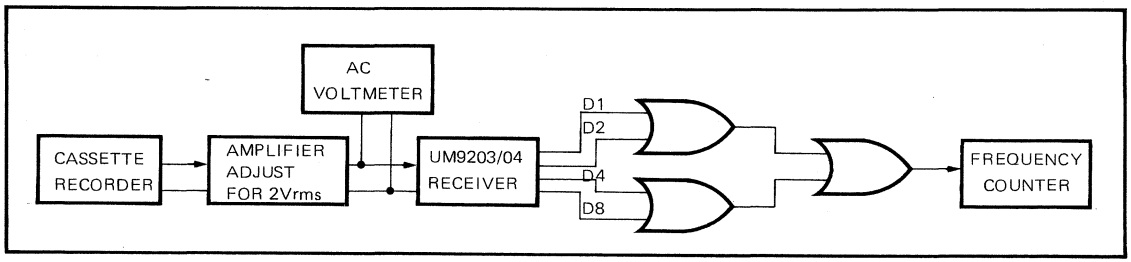


Figure 8 UM9203/04 Test Circuit

UMC

PRELIMINARY

UM93510 A/B/C

Speech Recording and Reproduction IC(with SRAM)

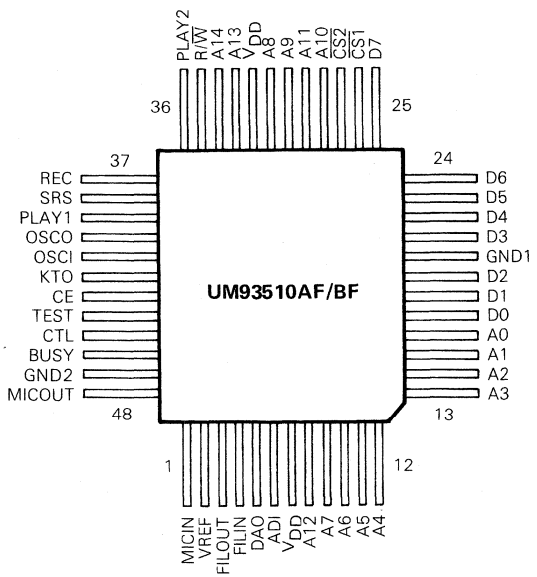
Features

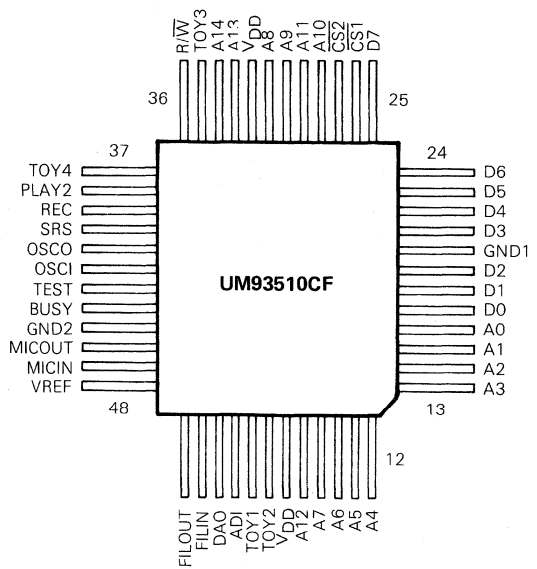
- Uses ADM algorithm to process voice data
- Uses three sampling rates (16K, 22K, 32K) selected by single pin (SRS)
- Useful in applications such as: answering machines, announcing phones and toys
- Metal mask option for answering machine or announce phone selection
- Data can be stored on SRAM or ROM:
  - Two 256K SRAMs for 32K sample rate
  - One 256K SRAM for 22K or 16K sample rate
  - One 256K SRAM and one 256K ROM for toy applications
- Activating the CE pin stops recording
- On-chip amplifier for sound recording
- On-chip band-pass filter for reproducing sound
- On-chip oscillation circuit for 3.579545 MHz ceramic oscillator
- 4.5V power supply using three 1.5V batteries
- Available in 48 pin flat package or in chip form

General Description

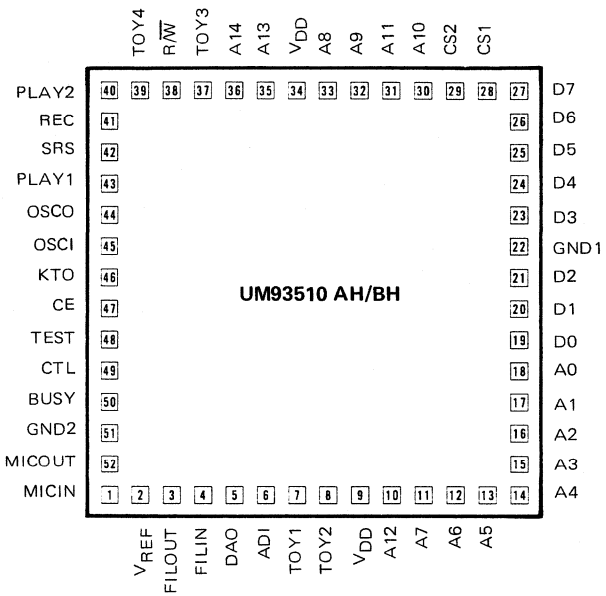
The UM93510 A/B/C is a speech recording and reproduction chip. It stores voice data on external 256K SRAMs. The primary use for the UM93510 A/B/C is in answering machines or announcing phones. It can also be used for toys. The 256K ROM should be partitioned into four parts for toy applications.

Pin Configurations

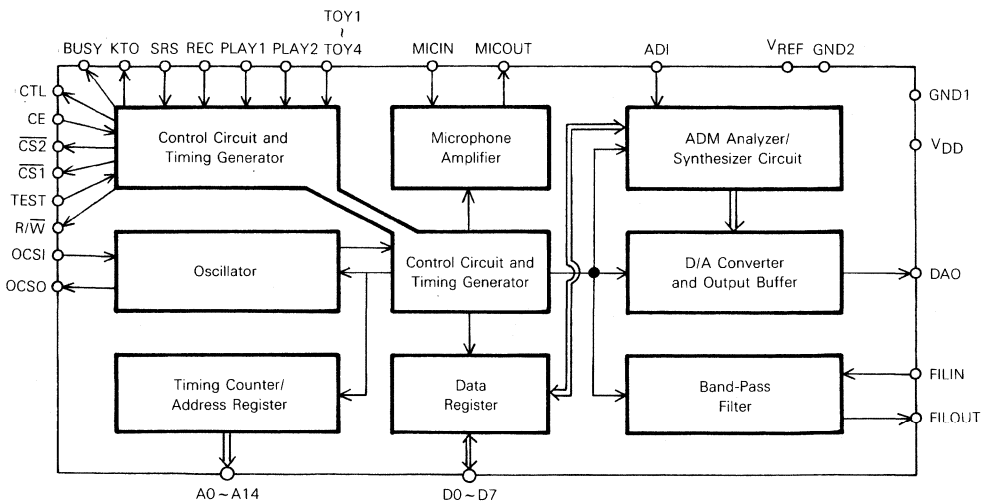




Pad Configuration



Block Diagram



Pin and Pad Description

Pin		Symbol	Pad	Description
A/B	C		AH/BH	
1	47	MICIN (I/P)	1	The inverting input terminal of the built-in microphone operational amplifier.
2	48	V_{REF} (O/P)	2	The bias voltage terminal of the built-in analog circuit. This pin is pulled to GND at standby state.
3	1	FILOUT (O/P)	3	The output pin of the built-in bandpass filter. The DC bias voltage of this pin is equal to 1/2 V_{DD} in playing mode and is pulled to GND in standby state.
4	2	FILIN (I/P)	4	The input terminal of the built-in bandpass filter for reproducing.
5	3	DAO (O/P)	5	The voice output terminal of the voice synthesizing circuit. Output signals have been biased to 1/2 V_{DD}. This pin is pulled to GND at standby state.
6	4	ADI (I/P)	6	The voice input terminal of the voice analysis circuit. Input signal must have been biased to 1/2 V_{DD}.
7 32	7 32	V_{DD} (I/P)	9 34	Positive power supply.
8 ~ 16 28 ~ 31 33 34	8 ~ 16 28 ~ 31 33 34	A0-A14 (O/P)	10 ~ 18 30 ~ 33 35 36	The address bus output pins.
17 18 19 21 ~ 25	17 18 19 21 ~ 25	D0-D7 (I/O)	19 20 21 23 ~ 27	The data bus input/output pins.
20	20	GND1 (I/P)	22	Digital circuit ground pin.
26 27	26 27	$\overline{CS1}$, $\overline{CS2}$ (O/P)	28 29	The chip selector output pins for 256K SRAM1 and SRAM2 (or ROM). If toy play is used, it is always to active $\overline{CS2}$.
35	36	R/$\overline{W}$ (O/P)	38	The read, write control output pin for SRAM.
36	38	PLAY2 (I/P)	40	The PLAY2 input pin is triggered manually. It is pulled low internally.
37	39	REC (I/P)	41	Record input trigger pin. Whenever this pin is triggered, the chip stops automatically under two conditions: (1) The SRAM memory is full (2) the CE pin has been pulled low. In the second case, the time for BUSY from HIGH to LOW is 0-1 second. (counts from the moment when the CE pin is switched to LOW) The delay time is not known, but depends on the current address. It is pulled low internally.

Pin and Pad Description (Continued)

<table>
<tr><th colspan="2">Pin</th><th rowspan="2">Symbol</th><th>Pad</th><th rowspan="2">Description</th></tr>
<tr><th>A/B</th><th>C</th><th>AH/BH</th></tr>
<tr><td>38</td><td>40</td><td>SRS
(I/P)</td><td>42</td><td>Sample rate selector pin for ADM algorithm. There are three different sample rates: 16 KHz, 22 KHz and 32 KHz. The relationship between SRS and sample rate is:

<table><tr><th>SRS</th><th>Sample Rate</th></tr><tr><td>high</td><td>32 KHz</td></tr><tr><td>low</td><td>22 KHz</td></tr><tr><td>open</td><td>16 KHz</td></tr></table></td></tr>
<tr><td>39</td><td>NA</td><td>PLAY1
(I/P)</td><td>43</td><td>The PLAY1 input pin is triggered by the ringing of the telephone. While high normally, it is pulled low when triggered. After the pin is triggered, the chip starts processing data after a delay of about 12 seconds for 22 KHz sample rate and 12.5 seconds for the 32 KHz sample rate and 16 KHz sample rates. If the ring time is less than 7.5 seconds, the trigger will not be successful and the chip will automatically enter the standby state. If the ring time is longer than 7.5 seconds but shorter than 12.5 seconds (or 12.0 seconds when the sample rate is 22 KHz), triggering will be successful and the chip will start to work. When this pin is pulled to GND, the current sourcing to GND is 20 μA (max.) at V_{DD} = 4.5V.</td></tr>
<tr><td>40
41</td><td>41
42</td><td>OSCI, OSCO
(I/P, O/P)</td><td>44
45</td><td>3.579545 MHz ceramic oscillator connecting pins.</td></tr>
<tr><td>42</td><td>NA</td><td>KTO
(O/P)</td><td>46</td><td>Key tone output pin. When the REC, PLAY2 pins are triggered or after BUSY pin from high to low (only in UM93510A/B & Chip form), this pin will send out a key tone. Duration and frequency are:

<table><tr><th>Sample rate</th><th>Tone frequency</th><th>Tone duration</th></tr><tr><td>32 KHz</td><td>500 Hz</td><td>112 ms</td></tr><tr><td>22 KHz</td><td>688 Hz</td><td>163 ms</td></tr><tr><td>16 KHz</td><td>500 Hz</td><td>224 ms</td></tr></table>
This pin is always pulled low, except during key tone period.</td></tr>
<tr><td>42</td><td>NA</td><td>CE
(I/P)</td><td>47</td><td>The chip enable input control pin. If CE is enabled. i. e., it can normally operate as described in the specification. If CE is low, it remains in a standby state, no matter which pin is triggered. If the CE pin is pulled low while operating, it enters the standby state immediately. It is internally pulled high. When this pin is switched to GND, the current sourcing to GND through this pin is 20 μA (max.) at V_{DD} = 4.5V.</td></tr>
<tr><td>44</td><td>43</td><td>TEST
(I/P)</td><td>48</td><td>Test input pin for testing mode. It is internally pulled low.</td></tr>
</table>

Pin and Pad Description (Continued)

Pin		Symbol	Pad	Description
A/B	C		AH/BH	
45	NA	CTL (O/P)	49	Provides output control to the telephone set. It is high only in PLAY1 Operation.
46	44	BUSY (O/P)	50	Output signal to indicate the chip is busy processing data. BUSY is high when the chip is active.
47	45	GND2 (I/P)	51	Analog and some digital circuit ground pin.
48	46	MICOUT (O/P)	52	The output terminal of the built-in microphone operational amplifier. Output signal has been biased to 1/2 V_{DD} and can be directly connected to ADI terminal. This pin can not have DC path to GND in standby state, or it will have DC power dissipation.
NA	5	TOY1 (I/P)	7	This pin is only available for TOY applications. (i. e. UM93510C). When triggered, this pin will cause the first quarter of the data on the 256K ROM to be played. It is pulled low internally.
NA	6	TOY2 (I/P)	8	This pin is only available for TOY applications. (i. e. UM93510C). When triggered, this pin will cause the second quarter of the data on the 256K ROM to be played. It is pulled low internally.
NA	35	TOY3 (I/P)	37	This pin is only available for TOY applications. (i. e. UM93510C). When triggered, this pin will cause the third quarter of the data on the 256K ROM to be played. It is pulled low internally.
NA	37	TOY4 (I/P)	39	This pin is only available for TOY applications. (i. e. UM93510C). When triggered, this pin will cause the last quarter of the data on the 256K ROM to be played. It is pulled low internally.

Notes: 1. The debounce time for all input control trigger pins is 23 ms for all sample rates.

2. The chip can not accept a new input trigger signal if any control pin has already been triggered. No new trigger signals can be accepted until the chip enters the standby state.
3. When the chip is used in an announce phone or an answering machine:
   a. If the sample rate is 32 KHz, two SRAMs are required to store the data. One SRAM can be used, but will only store eight seconds of data, then wait another eight seconds before stopping.
   b. If the sample rate is 16 KHz or 22 KHz, only one SRAM needs to be connected to $\overline{CS1}$. It will not activate $\overline{CS2}$.
4. When the chip is used in toy applications, the 32 KHz sample rate is not used to synthesize speech. One SRAM chip can be connected to $\overline{CS1}$ or one ROM chip to $\overline{CS2}$, or one SRAM chip to $\overline{CS1}$ and one ROM chip to $\overline{CS2}$.
5. NA: Not available
6. The difference between the UM93510 A and B is the CTL and KTO output timings shown in Timing Waveform(3).

Functional Description:

The UM93510 A/B/C is a voice processing and reproducing chip which can be used in both answering machine and toy applications. The input voice signals are processed into digital signals using the ADM (Adaptive Delta Modulation) algorithm. The digital data will be reproduced into analog voice signals when proper trigger conditions occur.

(a) UM93510 A/B

This chip can go into play mode by connecting the PLAY 2 pin to logical 1 level for a period more than 23 ms debounce time or by connecting the PLAY 1 pin to a logical 0 level for more than 7.5 sec. For answering machine or announce phone applications PLAY 1 is normally connected to a ringer detect circuit.

Note: The UM93510A will go into standby mode after the stored data is played while the UM93510B will enable the recorder for about 36 sec. The differences between A and B versions is shown in Timing Waveform (3).

(b) UM93510C

This chip can be triggered into play mode by either connecting PLAY 2 to logical 1 or connecting one of the TOY1, TOY2, TOY3, TOY4 to logical 1 level. The debounce time of the above pins is 23 ms.

The sample rate of 32K Hz, 22K Hz, 16K Hz can be selected by the SRS pin connecting to the HIGH, LOW, or FLOATING condition respectively. When the 32K Hz sample rate is selected two 256K SRAM should be used.

Absolute Maximum Ratings*

Power Supply Voltage . . . . . −0.3V to +6.0V
Apply Voltage on Any Pin . . . . . −0.5V to V_{DD} + 0.5V
Maximum Power Dissipation (at 25°C) . . . . . 500 mW
Operating Temperature (T_{OP}) . . . . . −20°C to +70°C
Storage Temperature (T_{STG}) . . . . . −55°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{DD}) . . . . . 4.5V to 5.5V
Input Voltage (V_{in}) . . . . . 0V to V_{DD}
Output Voltage (V_{out}) . . . . . 0V to V_{DD}

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional Operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 4.5V, V_{SS} = 0V, F_{OSC} = 3.579545 MHz, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating voltage	V_{DD}	4.0		5.5	V	
Supply Operating current	I_{dd}			4.0	mA	Oscillator running, all outputs unloaded
Standby Current	I_{sb}			2.0	μA	Oscillator not running, all outputs unloaded
Digital output sink current (1)	I_{do11}		0.5		mA	V_{ol} = 0.8V
Digital output source current (1)	$\|I_{do12}\|$		0.5		mA	V_{oh} = 2.4V
Resistor Load to get full swing of Analog output	R_{ALD}	15			KΩ	Test circuit (2)
Digital input voltage rating	V_{dil}			0.8	V	
	V_{dih}	2.4				
Digital output voltage rating	V_{dol}			0.8	V	I_{do11} = 0.5 mA
	V_{doh}	2.4				I_{do12} = 0.5 mA
Analog output voltage rating	V_{aol}	0.25		0.75	V_{DD}	R_L > 5 KΩ

Note: 1. Pins BUSY, CTL, $\overline{CS1}$, $\overline{CS2}$, R/$\overline{W}$, A0 – A14, D0 – D7
2. Pins FILOUT, DAO, MICOUT

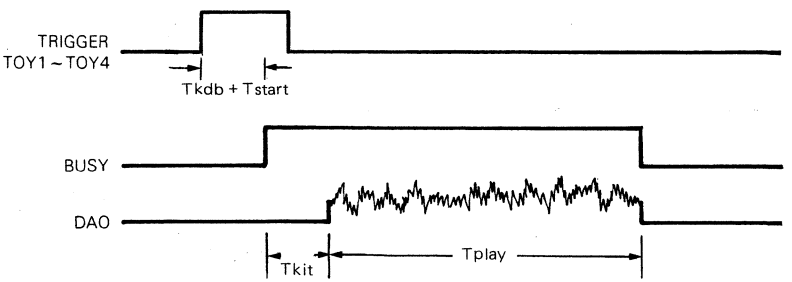
AC Electrical Characteristics

(V_{DD} = 4.5V, V_{SS} = 0V, F_{OSC} = 3,579545 MHz, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Key debounce time	Tkdb			23		mS
Key-in-tone duration	Tkit	sample rate 16K 22K 32K		 224 163 112		mS
Key-in-tone frequency	Fkit	sample rate 16K 22K 32K		 500 688 500		Hz
Period of announcement output	Tplay	256K or 512K memory maximum			16	Sec
Trigger period of incoming ringer signal	Tring	sample rate 16K 22K 32K		 12.5 12.0 12.5		Sec
Recording period for answer machine	Trec			36		Sec
Time between ringer signals	Trs				4	Sec
Oscillator start up time	Tstrart				50	mS

Timing Waveform

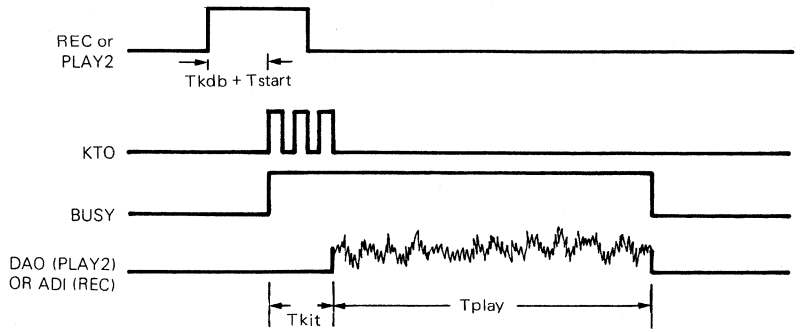
(1) Timing Waveform for TOY1, TOY2, TOY3, TOY4



Tkit: Key tone output period 224 ms or 163 ms

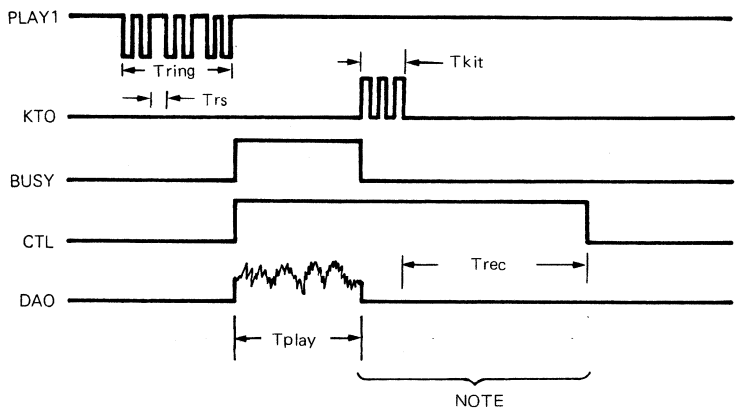
Tplay: Play or announcement period, 64K memory

(2) Timing Waveform for Recording and Reproducing (for UM93510A/B/C)



Tkit: Key Tone output Period 224 ms or 163 ms or 112 ms
Tplay: Play or Recording Period, maximum memory space: 256K or 512K
Note: The UM93510C, KTO pin is not available.

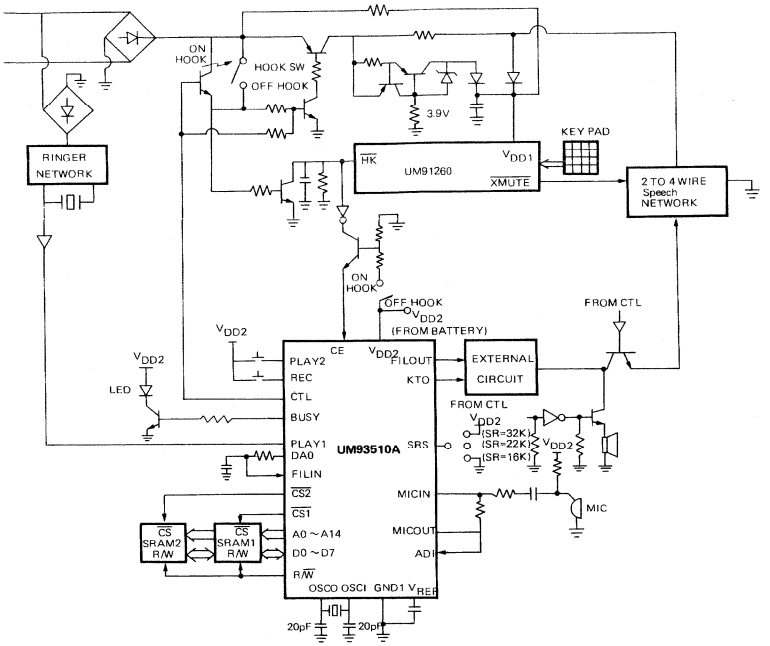
(3) Timing Diagram for Announcement-Recording (for UM93510A/B)



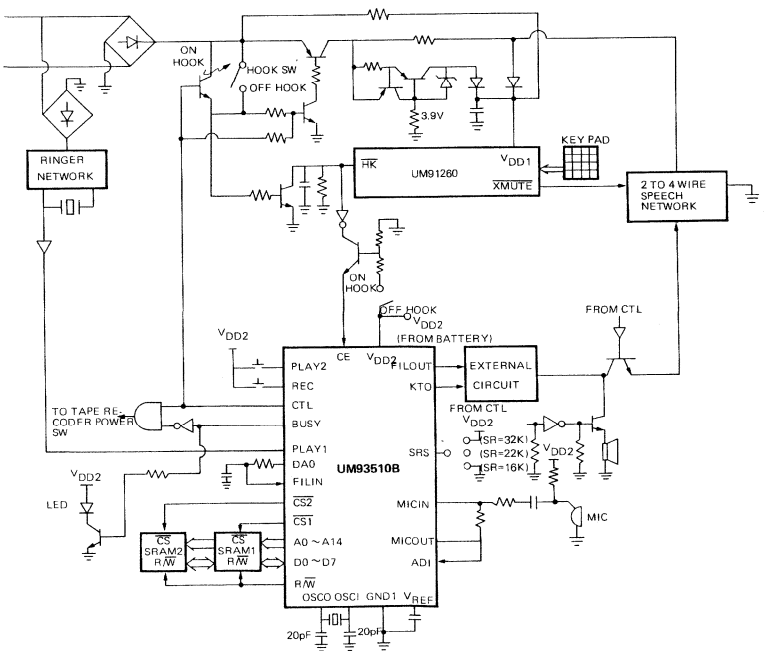
Tring: Trigger period of incoming ringer signal, 12 sec
Tkit : Key tone output period 224 ms or 163 ms or 112 ms
Tplay: Play or recording period, maximum memory space: 256K or 512K
Trec: Recording period for answering machine, 36 sec
NOTE: For announce phone, these states are replaced by standby state during this period. i. e. the KTO signal always stays at low, and the CTL signal has the same waveform as the BUSY signal.

Application Circuits

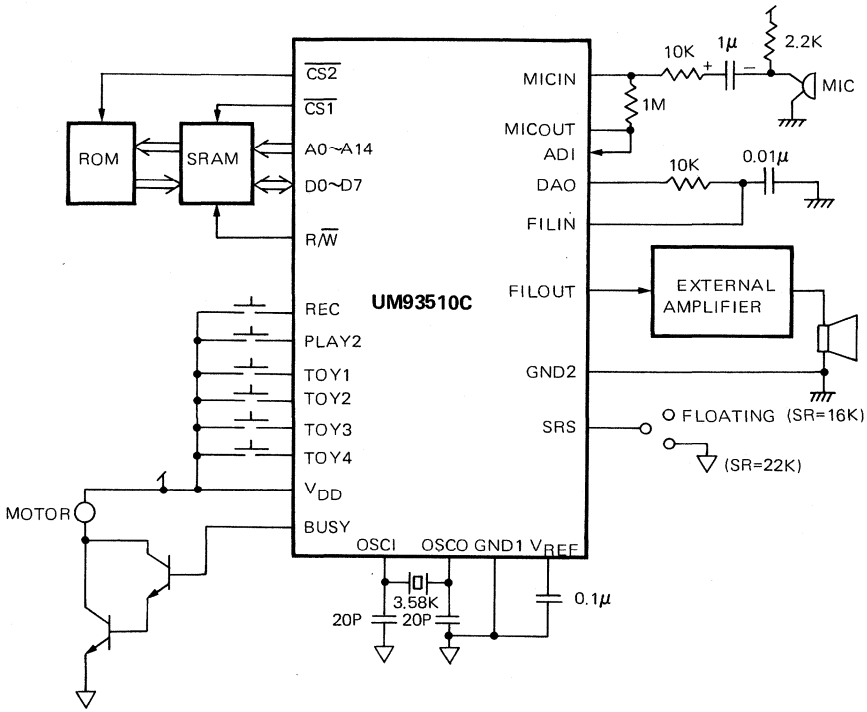
ANNOUNCE PHONE APPLICATION (UM93510A)



ANSWERING MACHINE APPLICATION (UM93510B)

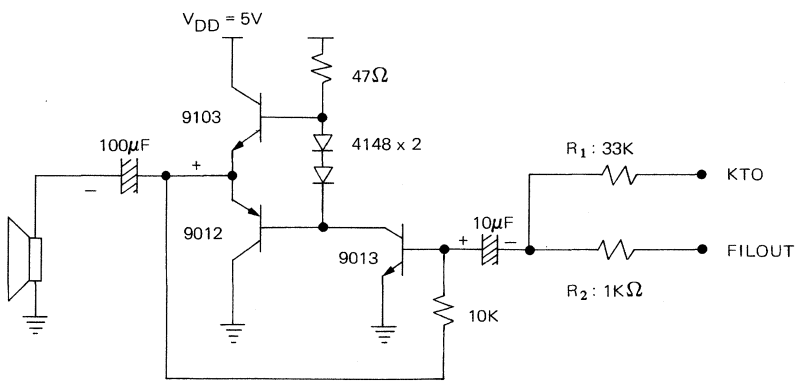


TOY APPLICATION

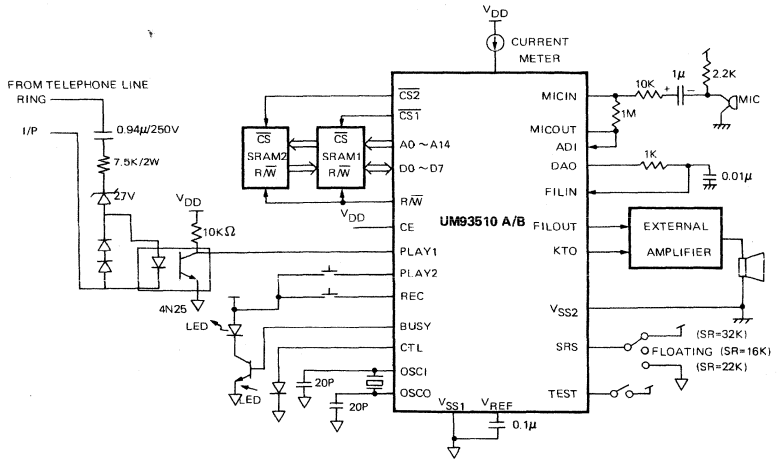


Notes: FILOUT is $\frac{1}{4}V_{DD} \sim \frac{3}{4}V_{DD}$ analog signal. Its output maximum current, Imax, is about 0.2 mA.

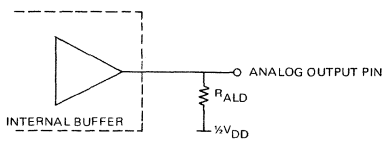
REFERENCE CIRCUIT FOR EXTERNAL AMPLIFIER



Test Circuit (1)



Test Circuit (2)



Ordering Information

Part No.	Application	Package Information
UM93510AF	Announcing phone	48-pin Flat pack
UM93510BF	Answering machine	48-pin Flat pack
UM93510CF	Toy Application	48-pin Flat pack
UM93510AH	Announcing phone & Toy	Chip Form
UM93510BH	Answering machine & Toy	Chip Form

UMC

UMC

UM9310

PRELIMINARY

Cordless Telephone Controller

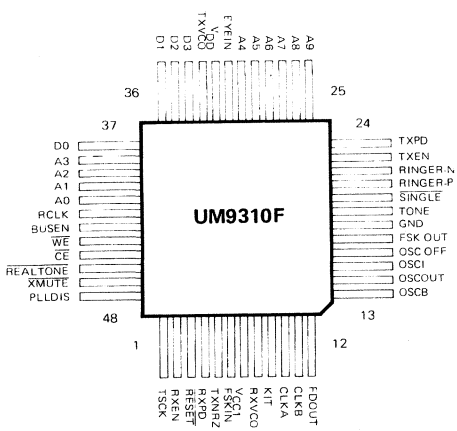
Features

- Two independent phase locked loop frequency synthesizers for transmitting and receiving
- 10 channels selectable
- Single frequency reference of 10.240 MHz
- Operating voltage of 3.3 to 5.5 volts
- On-chip 444.4 bps FSK modem
- Duplex data passage on pilot tone
- On-chip 1K SRAM expansion interface
- Microcontroller interface bus
- On-chip DTMF generator
- On-chip ringing tone output
- On-chip key-in tone output
- 48-pin flat package

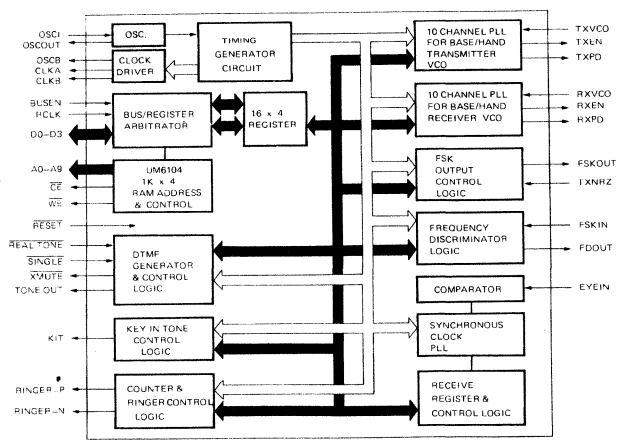
General Description

The UM9310 is a cordless telephone controller suitable for cordless telephone systems with automatic channel searching. It includes two independent PLL frequency synthesizers for the selection of communication channels. Up to ten channels can be selected. The UM9310 has a built-in modem which can be used to pass all control and status monitoring signals, such as ringing and dialing signal information between the handset unit and the base unit. For maximum flexibility in telecommunication applications, UM9310 also includes built-in DTMF tone, key-in tone, and ringing tone generators. All of the UM9310's operation can be controlled and monitored by accessing its 16 internal registers through a 4-bit data bus, which can be easily interfaced with a microprocessor or a microcontroller.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	TSCK	I	This pin is used for testing only and is internally pulled low.
2	RXEN	O	This pin functions as the receiver enable output. It follows the content of bit 1 of register 11.
3	$\overline{\text{RESET}}$	I	Chip reset. All registers are reset by this signal.
4	RXPD	O	Receiver VCO control pin. This pin sends a phase error detection signal to the receiver VCO. The frequency of the receiver VCO is controlled by the duty cycle of RXPD.
5	TXNRZ	O	Transmitter NRZ data is sent out through this pin.
6	FSKIN	I	The FSK signal is AC coupled to this input. The internal circuit of this pin is a waveshaper that converts the input FSK signal to a square wave which is sent to the frequency discriminator to determine the MARK or SPACE.
7	V_{DD2}		Positive power supply 2.
8	RXVCO	I	This input receives the receiver VCO frequency. The VCO signal is sharpened by a waveshaper and divided by two to act as the receiver PLL counter clock.
9	KIT	O	This is the KIT signal output. The KIT frequency is 1185 Hz.
10	CLKA	O	The frequency of this output is OSC/15 = 682.667 KHz. This output remains low as long as the $\overline{\text{RESET}}$ pin is low.
11	CLKB	O	The frequency of this output is OSC/3 = 3.413 MHz. This pin remains low as long as the $\overline{\text{RESET}}$ pin is low.
12	FDOUT	O	This pin is the frequency discriminator output. The FSK signal is converted to a mark or space voltage level determined by the frequency of FSK signal and output through this pin. This voltage is then filtered and sent to the EYEIN input.
13	OSCB	O	Oscillator buffer output.
14	OSCOUT	O	This is the oscillator output. A 10.24 MHz crystal and two capacitors should be connected between this pin and OSCIN to construct the oscillator circuit.
15	OSCIN	I	Oscillator input.
16	OSCOFF	I	This pin acts as the oscillator control pin. When this pin is high, the oscillator is disabled.
17	FSKOUT	O	This pin outputs the synthesized FSK signal. The synthesized waveform is a 10-time segment, 4-step sinusoid, and the data (MARK or SPACE) is controlled by TXNRZ.
18	GND		Signal ground.
19	TONE	O	This pin is the synthesized DTMF output. The row tone is a 20-time segment, 9-step sinusoid, while the column tone is 16-segment, 7-step sinusoid.

Pin Description

Pin No.	Symbol	I/O	Description
20	$\overline{\text{SINGLE}}$	I	This input controls the tone output. When this pin is low, a single tone is sent out rather than a row/column pair DTMF tone. The single tone produced for each key on the key pad is shown in the following: 1/R1 2/C2 3/R1 4/C1 5/R2 6/C3 7/R3 8/R3 9/R3 */R4 0/R4 #/R4
21	RINGERP	O	This pin is the ringer signal output.
22	RINGERN	O	Ringer signal output. This pin is the inverse of RINGERP.
23	TXEN	O	This pin functions as the transmitter enable output. It follows the content of bit 0 of register 11.
24	TXPD	O	Transmitter VCO control pin. This pin sends a phase error detection signal to the transmitter VCO. The frequency of the transmitter VCO is controlled by the duty cycle of TXPD.
25 – 30	A9 – A4	O	These pins output the external SRAM address.
38 – 41	A3 – A0	O	These pins output the external SRAM address.
31	EYEIN	I	This input receives the filtered output of FDOUT. It contains a comparator to determine the FSK signal as MARK or SPACE.
32	V_{DD}		Positive power supply.
33	TXVCO	I	This input receives the transmitter VCO frequency. The VCO signal is sharpened by a waveshaper and divided by two to act as the transmitter PLL counter clock.
34 – 37	D3 – D0	I/O	These pins are the data I/O pins of the external SRAM and registers.
42	RCLK	I	This input signal is used to count the input data nibble and acts as the clock of the data latch.
43	BUSEN	I	This input is the bus enable pin. Data access of UM9310 by external processor is enabled by activating this pin to high.
44	$\overline{\text{WE}}$	O	This output follows bit 3 of the first nibble data and is used to control read/write operation of external SRAM or internal registers.
45	$\overline{\text{CE}}$	O	During SRAM operation, this pin sends a low signal which is the inverse of the fourth clock of RCLK.
46	$\overline{\text{REALTONE}}$	I	If this pin is low during the DTMF signal output, the tone duration counter will be reset, and the DTMF signal will be sent out continuously.
47	$\overline{\text{XMUTE}}$	O	This pin is held low during the DTMF signal output.
48	PLLDIS	I	This pin is used for testing only and is pulled low internally.

Function Description

The functions and operations of UM9310 are controlled by sixteen internal 4-bit registers, which can be accessed by external microcomputer or micro-controller.

Registers R0 to R11 are used to handle the data communications performed by built-in 444.4 bps modem.

Output Registers – R0 to R3 (write-only):

These four registers can only be written by the microcomputer or micro-controller. When bit 0 of register 8 is set to 1, data written in these registers is sent out from FSKOUT according to the following format:

Start bits	R0	R1	R2	R3	Stop bits
011000	4 bits data	4 bits data	4 bits data	4 bits data	01

first bit sent out — last bit sent out

Input Registers – R4 to R7 (read-only):

These four registers are read-only registers which can be read through data buses D0 to D3. Once the start character embedded in the data stream input to the FSKIN pin is detected, these registers will start to buffer the data within the start and stop characters into R4 to R7 in the sequence of R4, R5, R6 and then R7.

Output Status Register – R8 (read/write):

Only bit 0 of this register is used. When bit 0 is set, the transmission of data within R0 to R3 is initiated. It will be cleared automatically after the data within R0 to R3 has been transmitted out.

Input Status Register – R9 (read/write):

Bit 0	Bit 1	Bit 2	Bit 3
R4 data available	R5 data available	R6 data available	R7 data available

R9 is used to indicate whether the data buffered in input registers R4 to R7 is available to be read by the microcontroller or not. The associated bit in register R9 is set as long as the data received by the corresponding registers are available. They must be reset by the microcontroller in order to receive the next set of data.

Signal Status Register – R10 (read-only):

In normal data receiving operations, bit 0 of R10 will be set only when the receiver is synchronous with the incoming data stream. It will be reset when the synchronous signal is lost or bit 2 or R11 is cleared.

Modem control Register – R11 (write-only):

Bit 0	Bit 1	Bit 2	Bit 3
Transmitter on	Demodulator on	Asynchronous receiver on	Hand/base mode select

When bit 0 is cleared, the FSK generator will be disabled and powered down, R8 will be cleared, and TXPD will be pulled low. The TXEN pin, which follows the state of bit 0, is used to control the external RF amplifier and TXVCO.

Bit 1 is used to control the operations of the data receiving circuit. When it is cleared, the discriminator will be disabled, the slice comparator will be powered down and RXPD will be pulled low. At all other times this circuit will operate normally. The RXEN pin, which follows the state of bit 1, can be used to control the external RF amplifier, mixer, IF, and RXVCO.

The data receiver for extracting the timing clock and data information from the data communications of the built-in modem can be disabled by resetting bit 2 to 0, which will in turn reset R10. Bit 2 of R11 must be set to 1 during normal receiving operation.

UM9310 can be operated in either a base or a handset unit by programming bit 3 of R11. When bit 3 is 0, base mode is selected. When bit 3 is 1, handset mode is selected.

Channel Select Register – R12 (read/write):

One of ten channels (each consisting of a pair of transmitting and receiving frequencies) can be selected by programming R11 in accordance with Table 1:

bit				Channel	Transmission and Reception Frequency (MHZ)			
				No.	Base Unit (bit 3, R11 = 0)		Hand Unit (bit 3, R11 = 1)	
3	2	1	0		transmit	receive	transmit	receive
0	0	0	1	1	46.610	38.975	49.670	35.915
0	0	1	0	2	46.630	39.150	49.845	35.935
0	0	1	1	3	46.670	39.165	49.860	35.975
0	1	0	0	4	46.710	39.075	49.770	36.015
0	1	0	1	5	46.730	39.180	49.875	36.035
0	1	1	0	6	46.770	39.135	49.830	36.075
0	1	1	1	7	46.830	39.195	49.890	36.135
1	0	0	0	8	46.870	39.235	49.930	36.175
1	0	0	1	9	46.930	39.295	49.990	36.235
1	0	1	0	10	46.970	39.275	49.970	36.275

Table 1: Channel Selection

The frequencies listed in this table are synthesized by the external VCO and the built-in divider.

DTMF Dial Digit Register – R13(read/write):

The DTMF tone is sent out through the TONE pin by programming R13 in accordance with Table 2:

bit 3	bit 2	bit 1	bit 0	DTMF tone ($\overline{\text{SINGLE}}$ = 1)	Single tone ($\overline{\text{SINGLE}}$ = 0)
0	0	0	1	1	R1
0	0	1	0	2	C2
0	0	1	1	3	R1
0	1	0	0	4	C1
0	1	0	1	5	R2
0	1	1	0	6	C3
0	1	1	1	7	R3
1	0	0	0	8	R3
1	0	0	1	9	R3
1	0	1	0	0	R4
1	0	1	1	*	R4
1	1	0	0	#	R4
1	1	0	1	inhibited	inhibited
1	1	1	0	inhibited	inhibited
1	1	1	1	inhibited	inhibited
0	0	0	0	reset	reset

Table 2

	Frequency (Hz)	Deviation (%)
R1	695.65	–0.19
R2	771.08	+0.14
R3	853.33	+0.16
R4	941.18	+0.02
C1	1212.12	+0.26
C2	1333.33	+0.20
C3	1481.48	+0.3

If the $\overline{\text{REAL-TONE}}$ pin is pulled low, the tone signal will be output continuously. Otherwise, the tone output will be of minimum tone duration, t_{MFD}, and will automatically follow an interdigit pause, t_{IDP}. t_{MFD} and t_{IDP} are 101 ms in duration. R13 will reset to 0000 once the tone signal is sent out, and can only be written after cleared to zero.

Ringer and Key-In Tone Register – R14(Write-only):

Bit 3	Bit 2	Bit 1	Bit 0
—	high freq. pair/ low freq. pair	ringer output enable	key-in tone output enable

When bit 0 is set to 1, an 1185 Hz Key-in tone is sent out from the KIT pin for t_{MFD}, the minimum tone duration. If bit 0 is set repeatedly with a period less than 101 ms, the Key-in tone will be sent out continuously. Bit 0 will automatically reset to 0 once the Key-in tone has been sent out.

The ringer will be inhibited if bit 1 is reset to 0. When bit 1 is sent to 1, UM9310 will output a ringer signal if R15 contains a non-zero value. The time duration of ringing equals 270 ms times the content of R15.

The ringer signal consists of two different frequency pairs. For each pair, there are two different frequencies sent with a change rate of 19.75 Hz. The selection of frequency pair is determined by bit 2 of R14 and is described in Table 3.

Bit 2	Ringing Frequency (Hz)
0 (high air)	1896/2370
1 (low pair)	474/592.5

Ringer Time Register – R15(read/write):

The time duration for ringing can be preset by programming R15, the ringer timer. R15 will count down at a rate of about 3.7 Hz. The RINGERP and RINGERN pins will output ringer signals with the time duration determined by R15. R15 will automatically count down to zero during ringing. When R15 counts down to zero, the ringer stops. It is necessary to reload R15 with a non-zero value for another ringing.

Absolute Maximum Ratings*

Power Supply Voltage 5.5V
Input Voltage 5.8V
Maximum power dissipation . . . . . 500 mW
Operating temperature . . . . . 0°C to 70°C
Storage temperature . . . . . –55°C to 150°C
Lead temperature . . . . . 256°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.3V, T_{OP} = 25°C, unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	3.3		5.5	V	
I_{OP}	Operating Current			1.5	mA	Receive only, Outputs unloaded
I_{STB}	Standby Current		3.0	5.0	μA	(1) chip reset (2) oscillator off
V_{IH}	Input High Voltage	0.8 V_{DD}	V_{DD}	V_{DD} +0.3		1 input
V_{IL}	Input Low Voltage	V_{SS}–0.3	V_{SS}	0.2 V_{DD}		0 input
I_{OL}	Output Sink Current	0.8			mA	V_{OL} = 0.5V
I_{OH}	Output Source Current	0.8			mA	V_{OH} = 2.8V
ZOUT	FSKOUT		5.0k		ohm	
	FDOUT		15.0k		ohm	
	Tone		3.0k		ohm	
	TXNRZ		10.0k		ohm	
Vref	EYEIN Pin Comparator Reference Voltage	0.625 V_{DD}			volt	
Cin	Input Capacitance			10.0	pF	
Cout	Output Capacitance			10.0	pF	
V_{OC}	Column Tone Output Amplitude	680	740	800	mV_{P-P}	V_{DD} = 2.5V R_{LOAD} = 10 KΩ
V_{OR}	Row Tone Output Amplitude	515	560	605	mV_{P-P}	V_{DD} = 2.5V R_{LOAD} = 10 KΩ
DIS %	Distortion		1	5	%	See Note
V_{VRC}	Valley of single row/ column Tone output		1.4		V	V_{DD} = 2.5V R_{LOAD} = 10 KΩ

Note: $DIS\% = \dfrac{100 \times (V_1^2 + V_2^2 + \ldots\ldots + V_n^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$

a. $V_1, \ldots V_n$ is the intermodulation or the harmonic frequency in 500 Hz to 3400 Hz band

b. V_{IL}, V_{IH} are the individual frequency components of the DTMF signal.

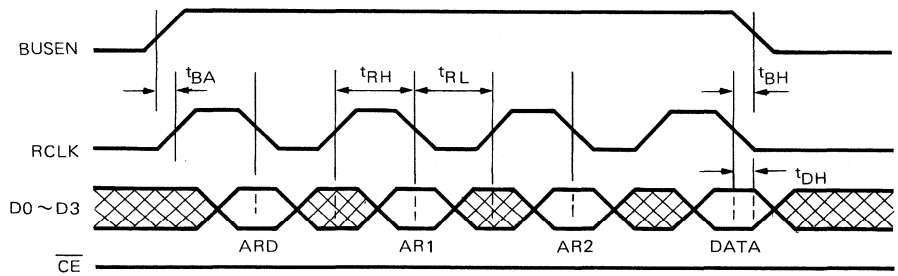
AC Electrical Characteristics (V_{DD} = 3.3V, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	RXVCO, TXVCO Pins Input Clock Rate			50.0	MHz	V_{P-P} > 0.3V
t_{BA}	Lead Time for Bus Enable Before Access	25			ns	
t_{BH}	Hold Time for Bus Enable After Access	25			ns	
t_{RH}	RCLK Clock High Duration	400			ns	
t_{RL}	RCLK Clock Low Duration	600			ns	
t_{DS}	Data Set Up Time	25			ns	
t_{MFD}	Minimum Tone Duration		101		ms	
t_{IDP}	Minimum Interdigit Pause		101		ns	
t_{DH}	Data Hold Time	0			ns	

Timing Waveform

(1) In order to operate properly as described previously for UM9310, the data access of internal registers and/or external SRAM should be programmed in accordance with the timing waveforms shown in Fig. 1.

(a) Microcontroller READ/WRITE data FROM/TO register:

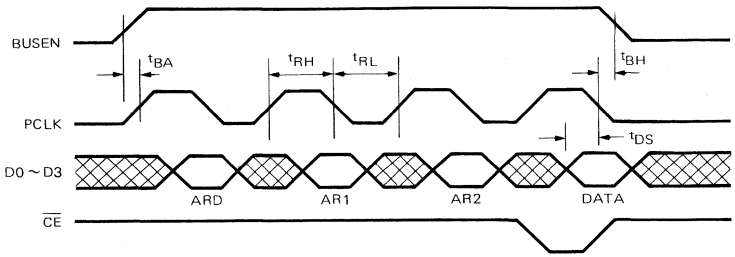


Note:

	BIT 3	BIT 2	BIT 1	BIT 0	
AR0	$\overline{WE}$	RSEL	–	–	RSEL = "1" = V_{DD}
AR1	–	–	–	–	$\overline{WE}$ = "0" (WRITE)
AR2	A3	A2	A1	A0	= "1" (READ)
DATA	D3	D2	D1	D0	

Figure 1(a)

(b) Microcontroller WRITEs to SRAM



Note:

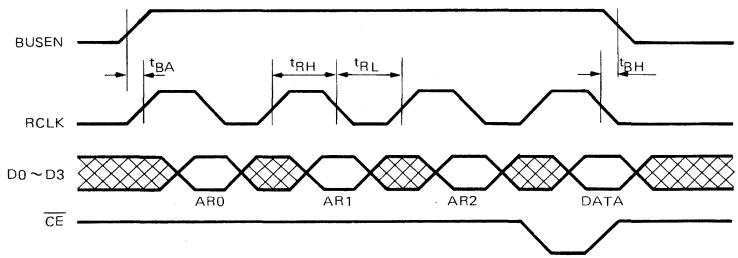
(1)

	BIT 3	BIT 2	BIT 1	BIT 0	
AR0	$\overline{WE}$	RSEL	A9	A8	RSEL = "0"
AR1	A7	A6	A5	A4	$\overline{WE}$ = "0" (WRITE)
AR2	A3	A2	A1	A0	
DATA	D3	D2	D1	D0	

(2) The SRAM interface timing is according to UM6104.

Figure 1(b)

(c) Microcontroller READs data from SRAM

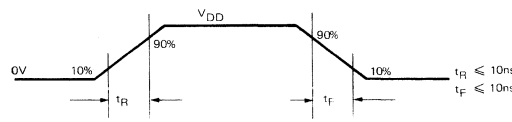


Note:

	BIT 3	BIT 2	BIT 1	BIT 0	
AR0	$\overline{WE}$	RSEL	A9	A8	RSEL = "0"
AR1	A7	A6	A5	A4	$\overline{WE}$ = "1" (READ)
AR2	A3	A2	A1	A0	
DATA	D3	D2	D1	D0	

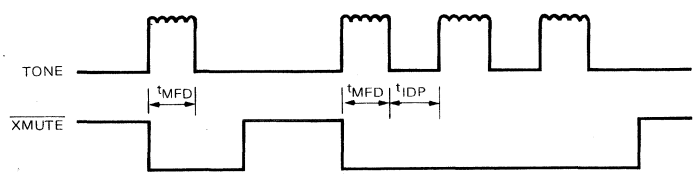
Figure 1(c)

Note: 1. Input Waveform limitations:



2. The address and/or data are latched at the falling edge of RCLK.

(2) The timing relation of TONE and $\overline{XMUTE}$ output is plotted in the following diagram.



Application Circuit

The application circuits are plotted in Figure-2, 3. Figure-2 is the overall block diagram for practical application. However, Figure-3 only contains part of the implementation circuit of Figure-2.

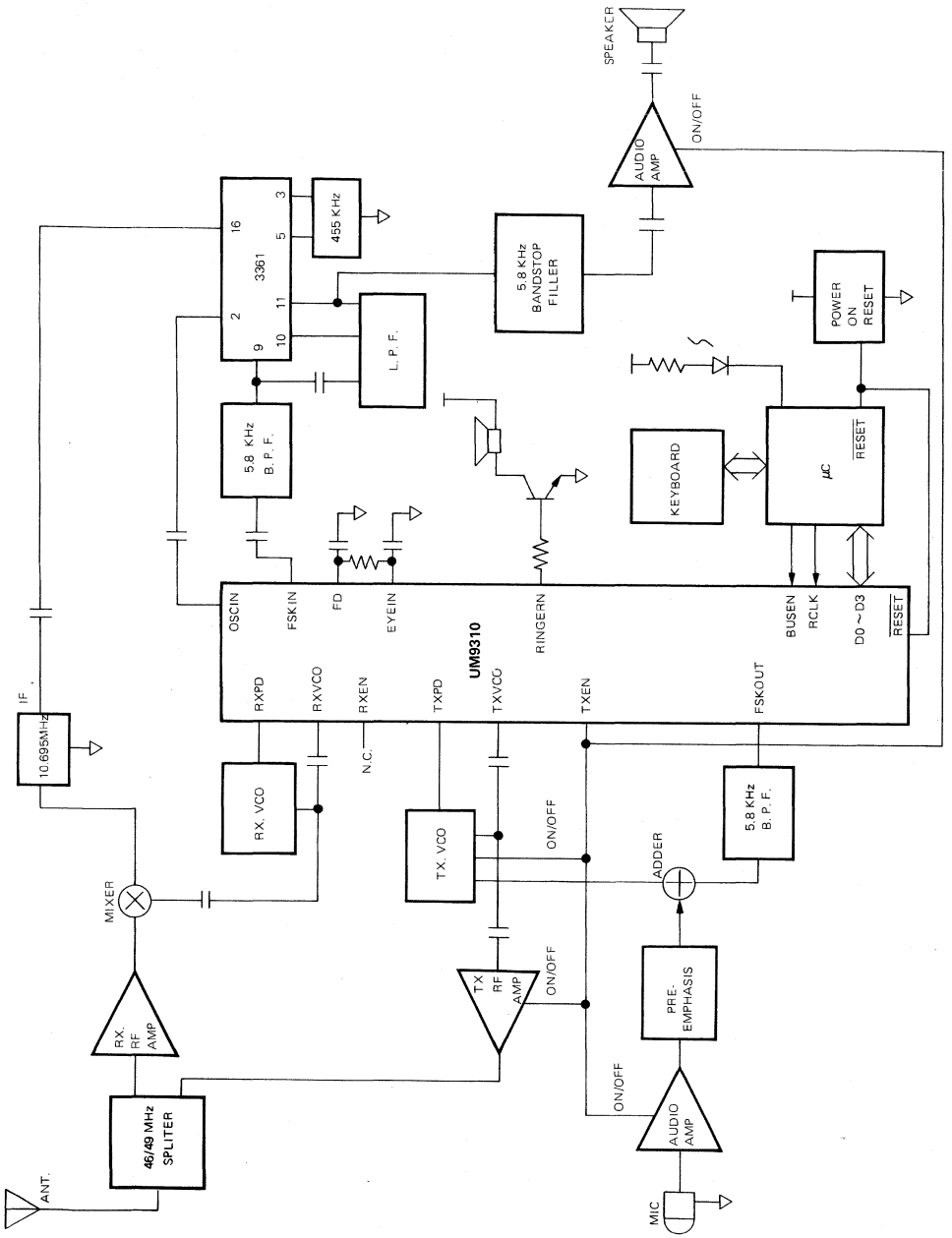


Figure-2(a) Block Diagram of the Cordless Telephone for Handset Unit

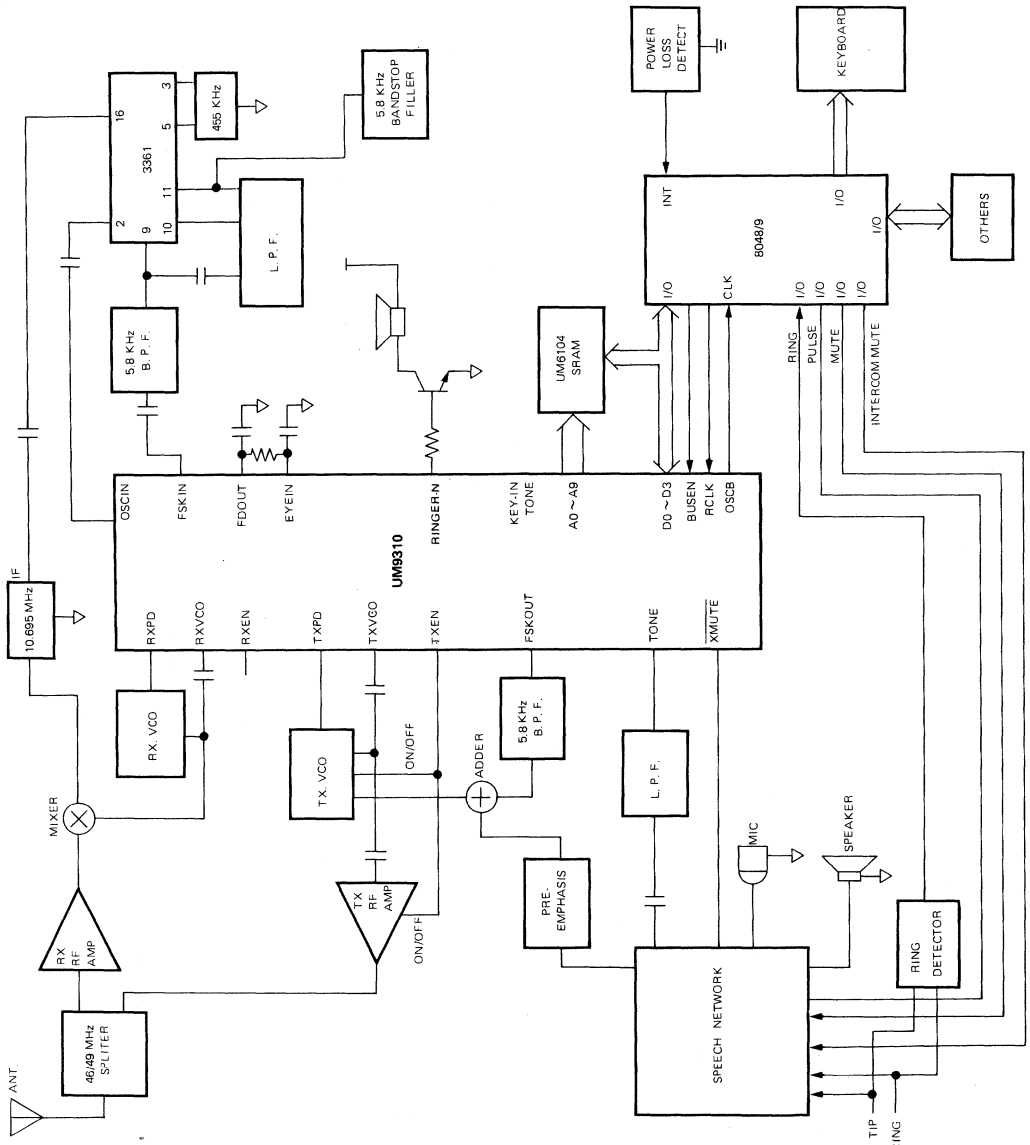


Figure-2(b) Block Diagram of the Cordless Telephone for Base Unit

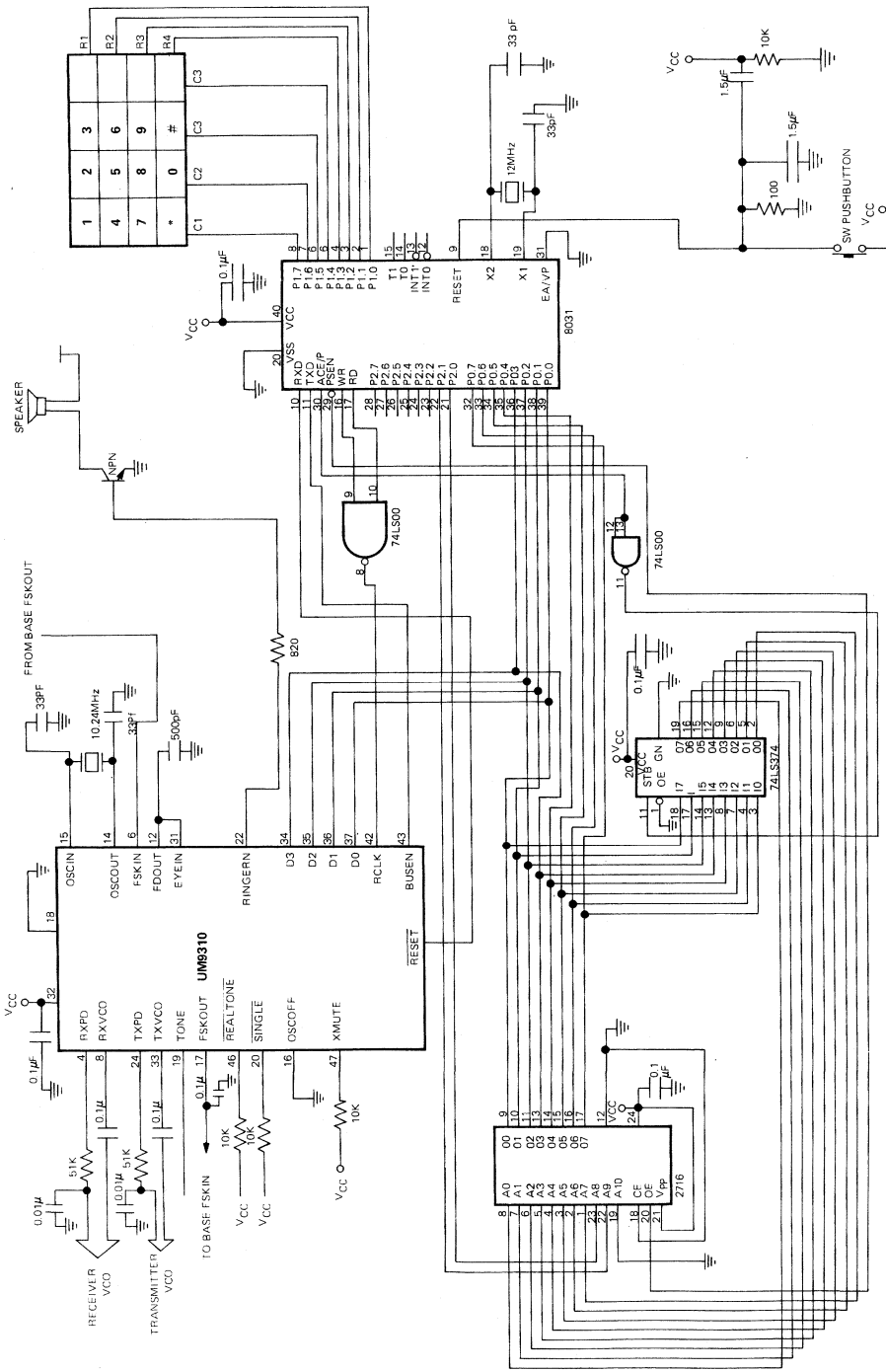


Figure-3(a) Implementation of Handset Unit (contains only part of Figure-2(a))

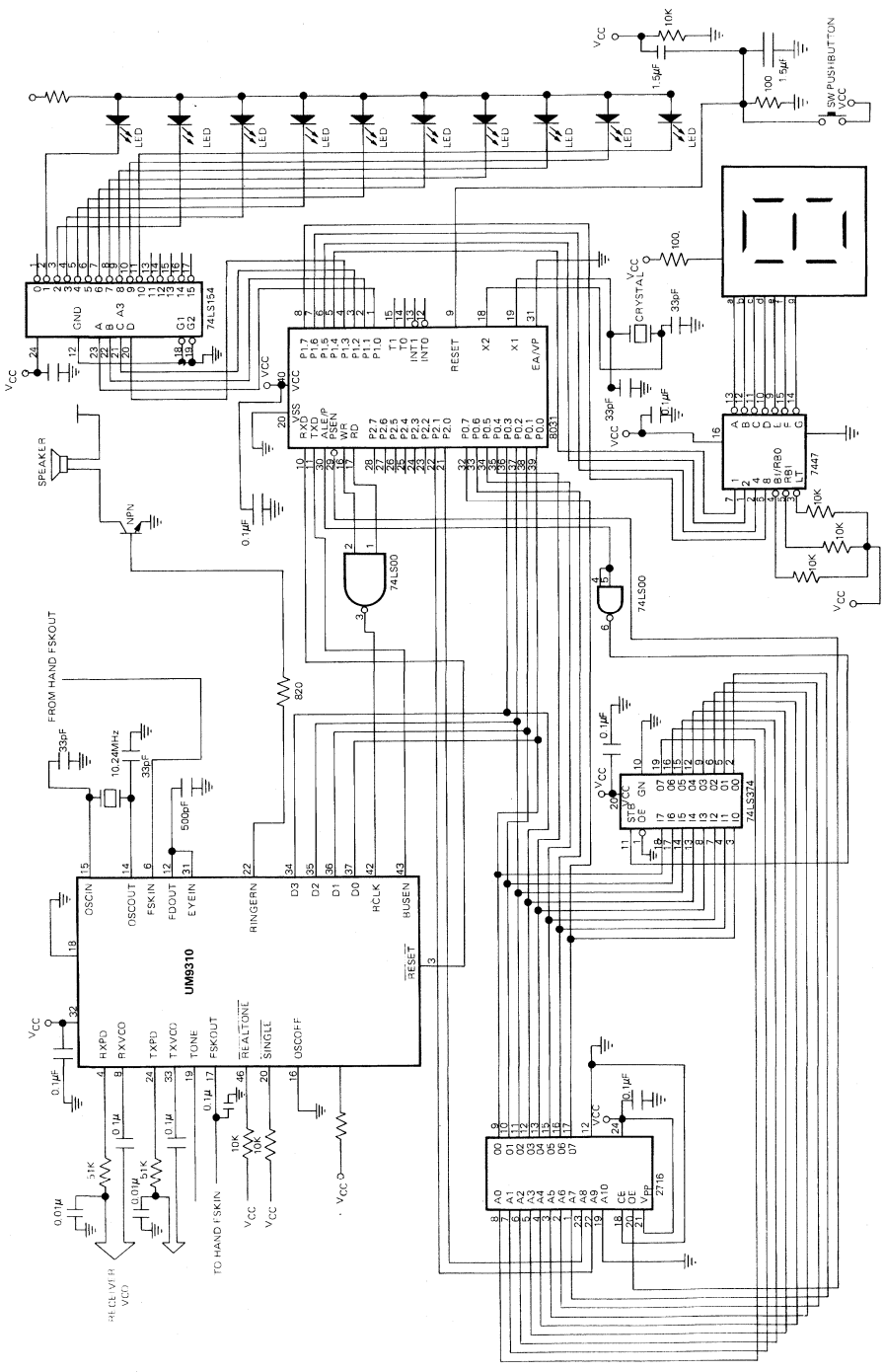


Figure-3(b) Implementation of Base Unit (contains only part of Figure-2(b))

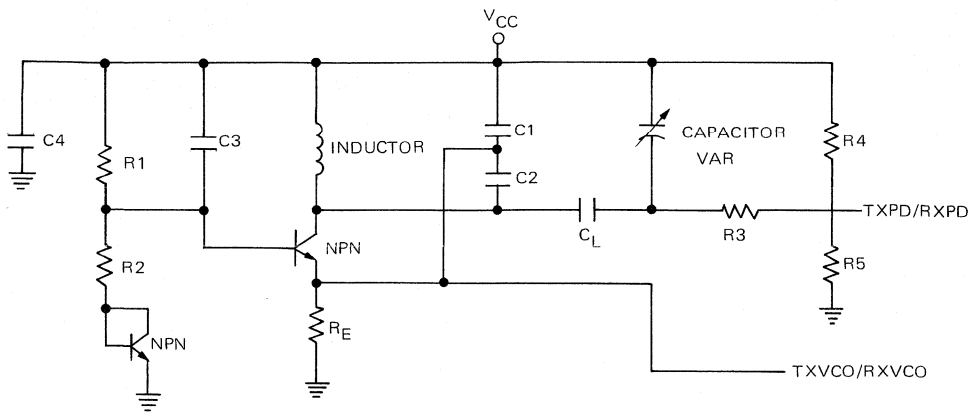


Figure-3(C) Implementation of The VCO circuit

UMC

PRELIMINARY

UM93520A/B

Speech Recording and Reproduction IC (with DRAM)

Features:

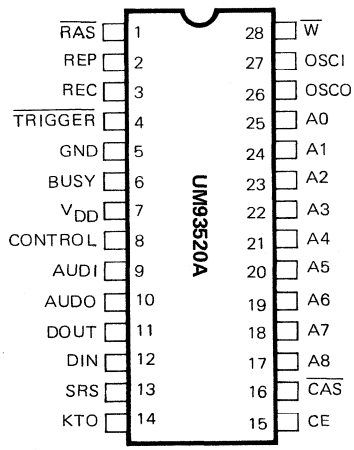
- Uses ADM algorithm to process voice data
- Built-in DRAM refresh circuit
- Three selectable sampling rates:
  UM93520A with one 256K DRAM: 16 KHz or 22 KHz by pin option
  UM93520B with two 256K DRAMs: 32 KHz
- On-chip oscillator for 3.579545 MHz crystal oscillator
- Single 5-volt power supply
- Available in 28 pin DIP (UM93520A/B) or 48-pin flat package (UM93520AF/BF)

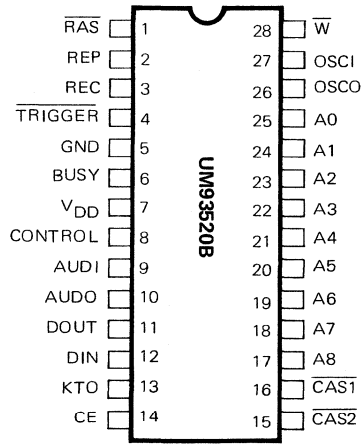
General Description

The UM93520A/B is a single-chip CMOS LSI for voice recording and reproducing. This chip is especially suitable for use as the recording and playback element of an answering machine. The design of this chip is based on Adaptive Delta Modulation (ADM) technology. Voice data is recorded and stored on 256K DRAMs. Each 256K DRAM can store 16 seconds of voice data at 16KHz sampling rate, 11.2 seconds at 22KHz sampling rate and 8 seconds at 32KHz sampling rate.

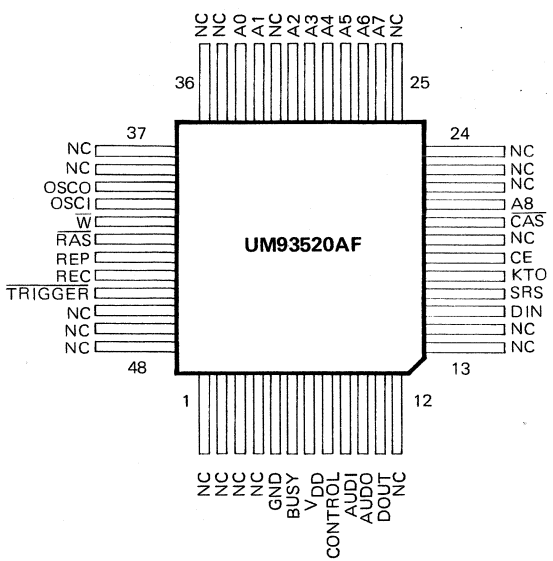
Pin Configurations

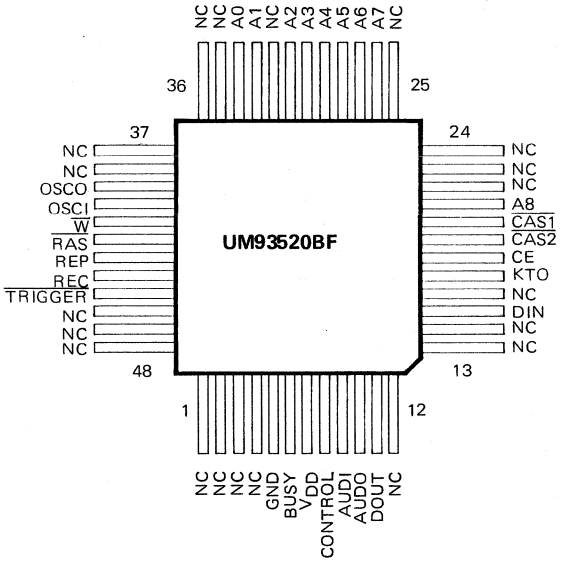
1. 28-pin DIP



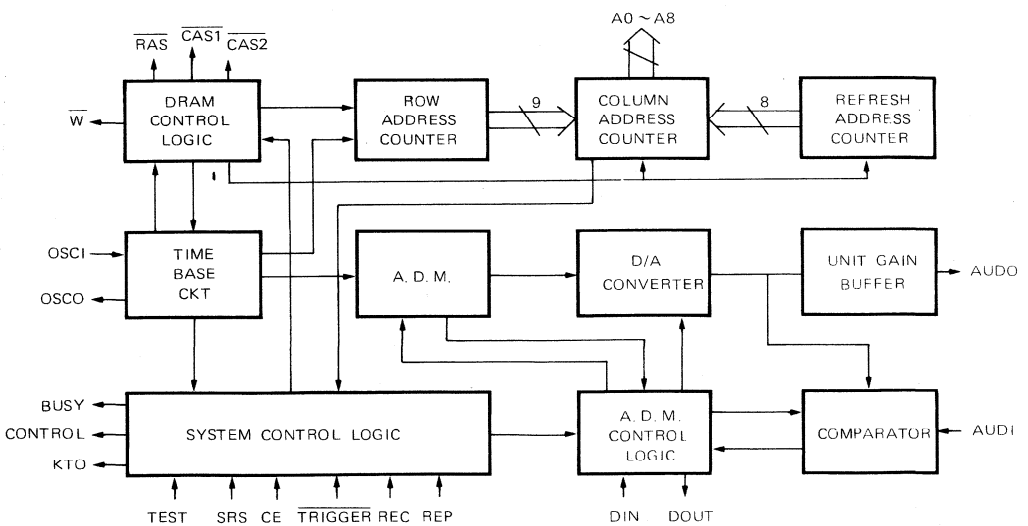


2. 48-pin flat package





Block Diagram



Pin Description

Pin No.		Symbol	I/O	Description
UM93520A (UM93520AF)	UM93520B (UM93520BF)			
1 (42)	1 (42)	$\overline{RAS}$	O	Row address strobe output pin. Connected to the $\overline{RAS}$ pin of the external DRAMs.
2 (43)	2 (43)	REP	I	Reproduction trigger input pin. Note: RECORD and REP inputs are debounced internally. The debouncing time is typically 300 ms. It's internally pulled low. High activated.
3 (44)	3 (44)	REC	I	Recording trigger input pin. It's internally pulled low. High activated.
4 (45)	4 (45)	$\overline{TRIGGER}$	I	Accepts a ring signal of 10.75 sec. duration and enables the chip if no one answers the phone. It's low activated, and internally pulled high.
5 (5)	5 (5)	GND		Ground pin.
6 (6)	6 (6)	BUSY	O	Recording/Reproduction state indication output pin. This output will stay high during the recording/reproduction state.
7 (7)	7 (7)	V_{DD}		Power supply +5V. (typ.)
8 (8)	8 (8)	CONTROL	O	Control output pin for tape recorder, high activated.
9 (9)	9 (9)	AUDI	I	Voice input pin for the recorded analog signal.
10 (10)	10 (10)	AUDO	O	Synthesized voice output pin.
11 (11)	11 (11)	DOUT	O	Data output pin. Connected to data input pin of the external DRAMs.
12 (15)	12 (15)	DIN	I	Data input pin. Connected to data output pin of the external DRAMs.
13 (16)		SRS	I	Sample rate select input pin. Connected high, sampling rate is 16 KHz. Connected low, sampling is 22 KHz.
14 (17)	13 (16)	KTO	O	Keytone output pin. The KTO pin is used for keytone output. If SRS is high, keytone is 500 Hz. If SRS is low, keytone is 699 Hz.
15 (18)	14 (18)	CE	I	Chip enable pin. High activated. It's internally pulled high. When pulled low, it means "reset the chip"
16 (20)		$\overline{CAS}$	O	Column address strobe output pin. Connected to $\overline{CAS}$ pin of the external DRAM.
	16 (20)	$\overline{CAS1}$	O	Column address strobe output pin. Connected to $\overline{CAS}$ pin of the external DRAM 1.
	15 (19)	$\overline{CAS2}$	O	Column address strobe output pin. Connected to $\overline{CAS}$ pin of the external DRAM 2.

Pin Description (Continued)

Pin No.		Symbol	I/O	Description
UM93520A (UM93520AF)	UM93520B (UM93520BF)			
17 – 25 (21, 26-31, 33, 34)	17 – 25 (21, 26-31, 33, 34)	A8 – A0	O	Address outputs pins to DRAMs.
26 (39)	26 (39)	OSCO		These two pins are for 3.579545 MHz crystal oscillator circuit.
27 (40)	27 (40)	OSCI		
28 (41)	28 (41)	$\overline{W}$	O	Write pulse output pin. Connects to $\overline{W}$ pin of the external DRAMs.

Note: Pins 1, 2, 3, 4, 12, 13, 14, 19, 22, 23, 24, 25, 35, 36, 37, 38, 46, 47, and pin 48 of UM93520AF or UM93520BF are NOT CONNECTED pins.

Absolute Maximum Ratings *

Supply Voltage (V_{DD}) . . . . . –0.3V to 6V

Input Voltage (V_{IN}) . . . . . –0.3V to V_{DD} + 0.3V

Output Voltage (V_{OUT}) . . . . . –0.3V to V_{DD} + 0.3V

Operating Temperature (T_{OP}) . . . . . –40°C to +125°C

Storage Temperature (T_{STG}) . . . . . –40°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5V ± 10%, T_A = 25°C, F_{OSC} = 3.579545 MHz) unless otherwise specified

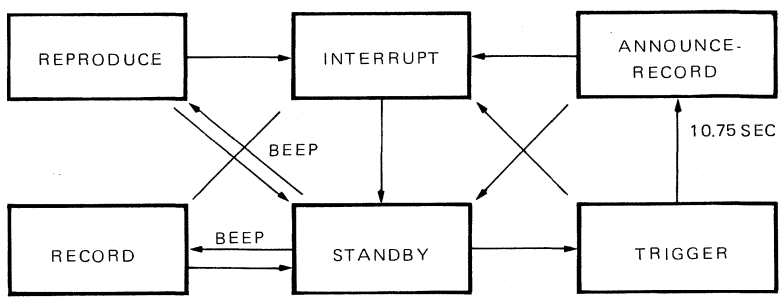
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{DD}	Standby Current		0.2	1	mA	Output unloaded Input not triggered
I_{OL}	Output sink current (Control, Busy)		9		mA	V_{OL} = 0.8V
I_{OH}	Output source current (Control, Busy)		9		mA	V_{OH} = 2.4V Note: This is an absolute value
V_{OA}	Audio output amplitude		2.2		V_{PP}	R_L = 1Kohm
V_{IH}	Input Voltage	2.4			V	
V_{IL}				0.8		

AC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, F_{OSC} = 3.579545 MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{WR}	$\overline{RAS}$ pulse width		3.9		μs	Sampling Rate = 32 KHz
			3.9			Sampling Rate = 16 KHz
			2.8			Sampling Rate = 22 KHz
t_{WC}	$\overline{CAS}$ pulse width		1.9		μs	Sampling Rate = 32 KHz
			1.9			Sampling Rate = 16 KHz
			1.4			Sampling Rate = 22 KHz
t_{TRIG}	Trigger Time		10.75		sec.	For any sampling Rate
t_{REP}	Reproduction and recording time		16		sec.	Sampling Rate = 32 KHz
			16			Sampling Rate = 16 KHz
			11.2			Sampling Rate = 22 KHz
t_{TREC}	Tape recording time		30.75		sec.	For any sampling Rate
f_{KTO}	KTO frequency recording time		1000		Hz	Sampling Rate = 32 KHz
			500			Sampling Rate = 16 KHz
			699			Sampling Rate = 22 KHz
t_{KTO}	KTO duration time		0.5		sec.	For any sampling Rate
t_{MINR}	Valid pulse width	280			ms	Debouncing time for REC., REP., CE. and $\overline{TRIGGER}$ pins

Functional Description & Timing Diagrams

1. The operating sequence for recording and reproduction is shown below:



2. Standby

The following conditions will cause the chip to enter the standby state:

1. Power on.
2. Completion of operations in the record, reproduce or announce-record states.
3. The cause of an interrupt is cleared.

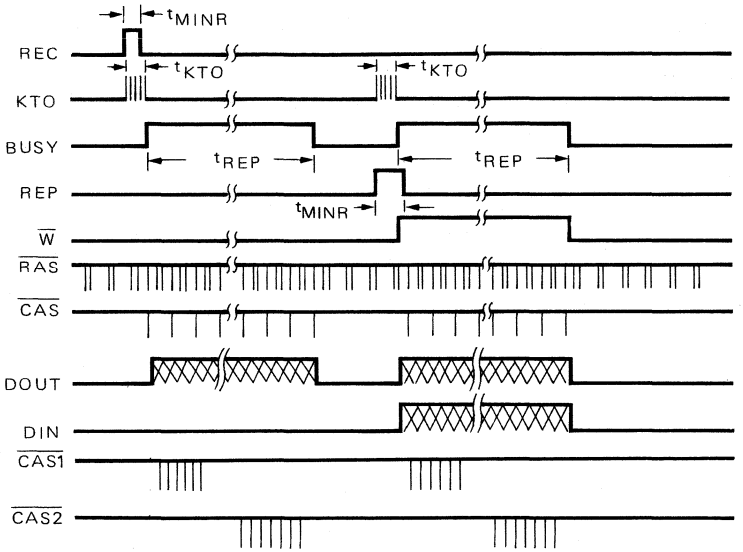
3. Recording and reproducing

Before the announce/recording sequence operates normally, an announcement must have been recorded in advance from within the record state. This can be achieved by pulling the REC pin to high, which will immediately cause a beep to output for 0.5 seconds from the KTO pin.

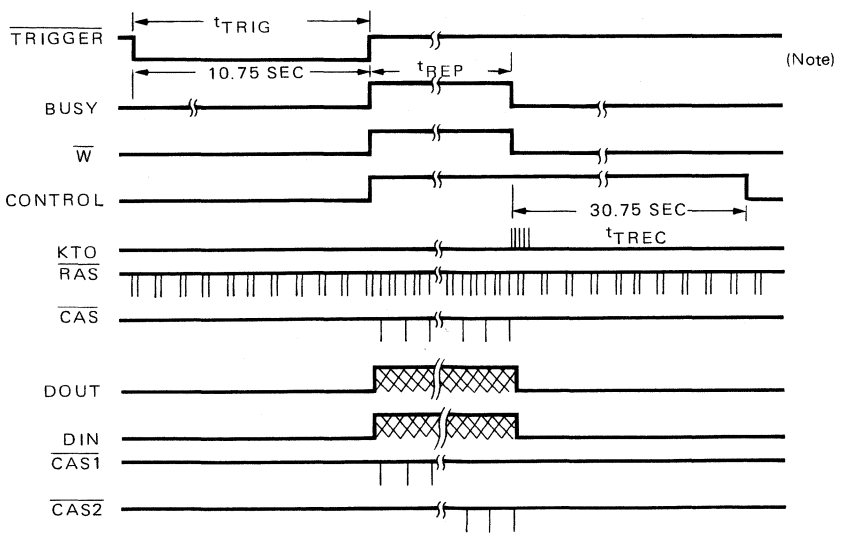
To check an announcement that was recorded previously in the reproduction state, the REP pin can be pulled high and, as in the record state, a beep will be transmitted and the announcement will be sent out from AUDO.

Both the record and reproduction states can be interrupted by dropping the CE pin to low, which will stop recording or reproduction. The frequency of the beep and the maximum recording time depend on the sampling frequency, as follows:

Sample Rate	16K	22K	32K
Beep (f_{KTD})	500 Hz	699 Hz	1 KHz
Time (t_{REP})	16s	11.2s	16s



4. Announcing and recording



4. Announcing and recording

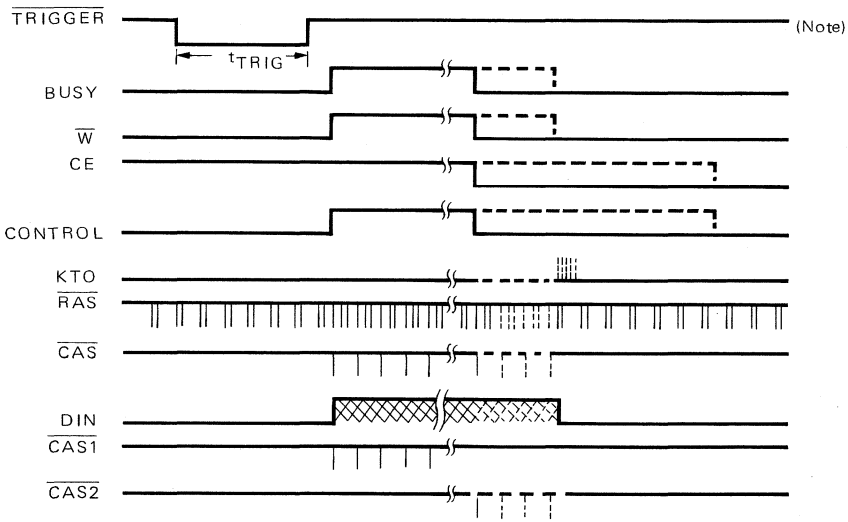
The Announce/Record state is triggered when the ring signal from the subscriber loop comes in for more than 10.75 seconds without interruption. In this state, any previously recorded announcement will be sent out, with the BUSY and CONTROL pins going high and a tape recorder enabled to record a maximum of 30.75 seconds of voice data. In addition, a beep will be sent out as shown in the diagram below.

5. Interrupt

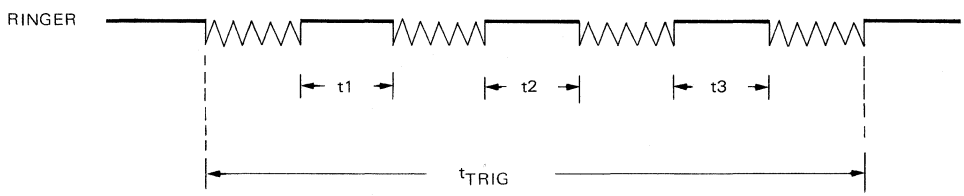
There are two ways to enter the interrupt state:

1. Dropping the CE pin from high to low.
2. The absence of a trigger signal for more than four seconds during the trigger state.

Once a trigger signal is accepted, however, it can no longer be interrupted, even if the caller hooks the telephone handset.

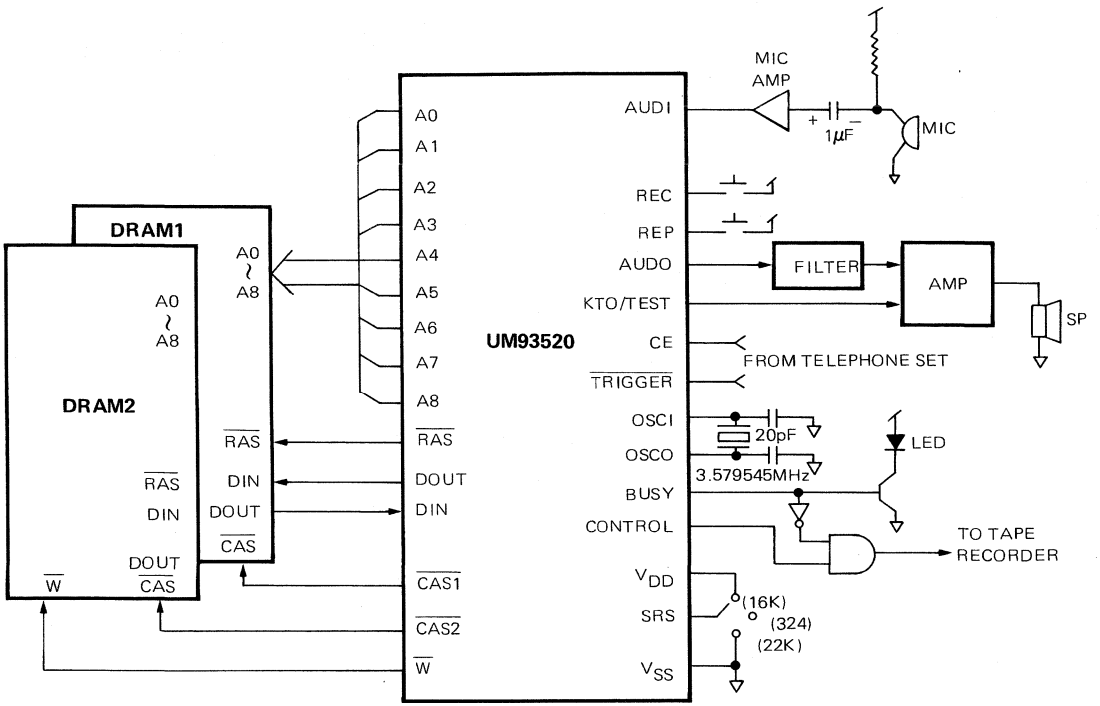


Note: The TRIGGER pin is normally connected to the telephone ringer detector t_{TRIG} means the time duration after the first signal is on. If pause time between two ringer signals exceeds 4 seconds, the trigger duration will reset to zero. The trigger shown below works, where $t_{TRIG} \geqslant 10.75$ seconds and pause time (t1, t2, t3) must be less than 4 seconds.



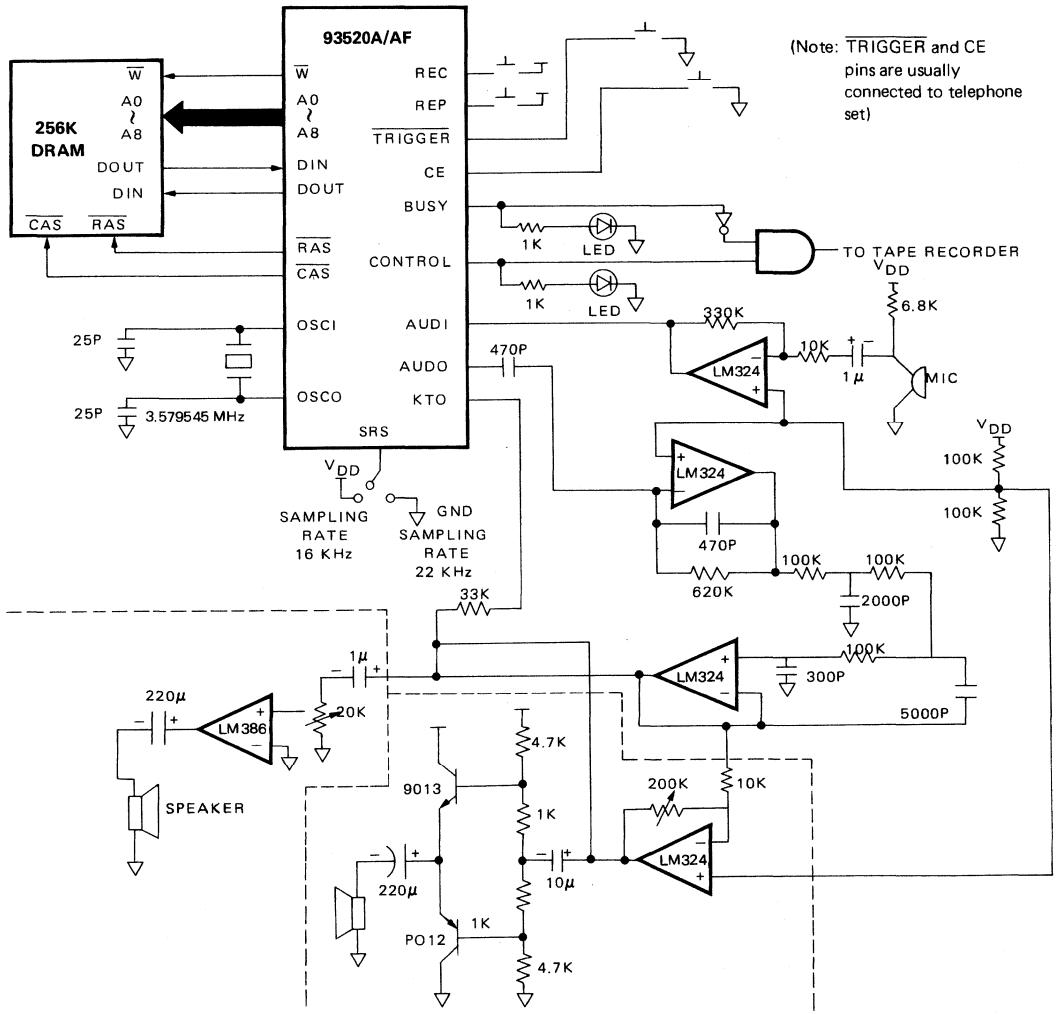
Applications Circuits

(A) General



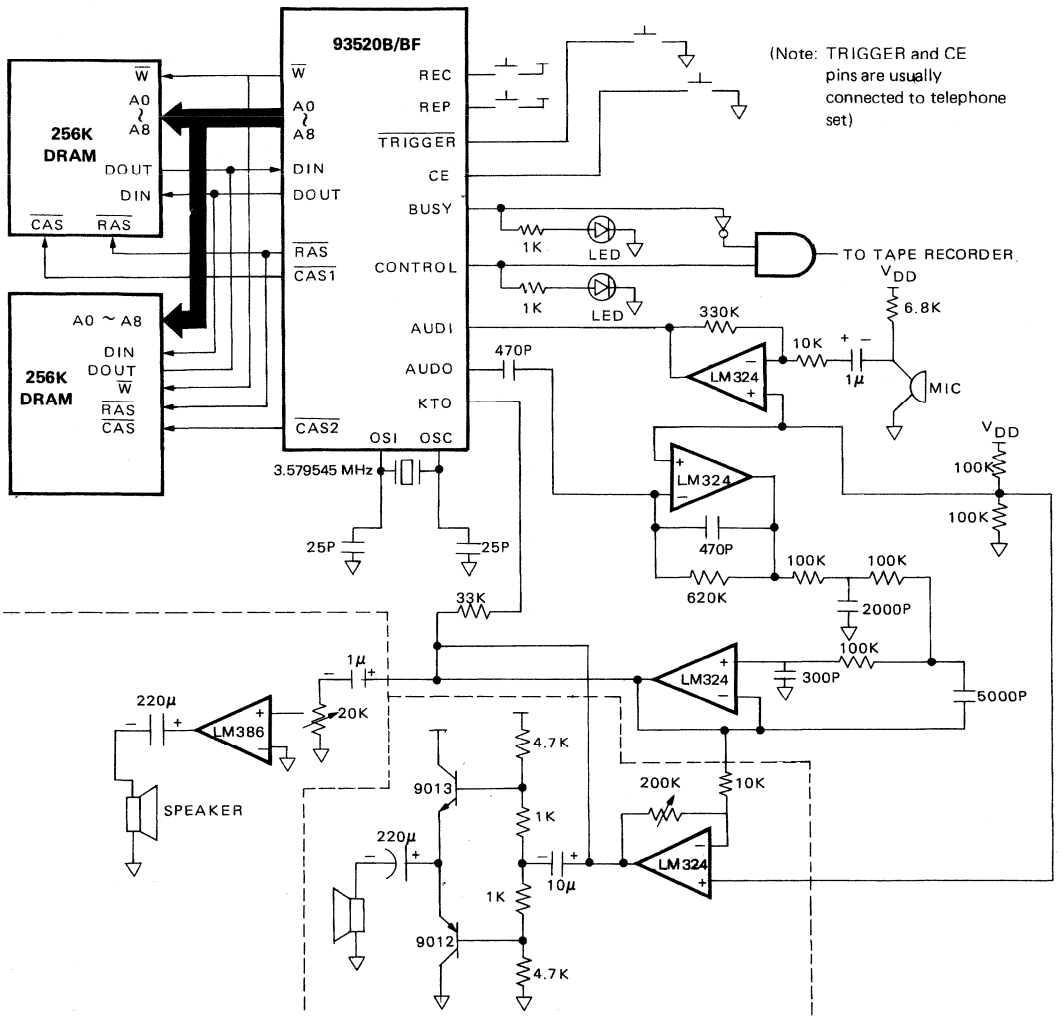
Applications Circuits: (Continued)

(B) UM93520A/UM93520AF



Applications Circuits: (Continued)

(C) UM93520B/UM93520BF



Ordering Information

Part No.	Sampling Rate	DRAM	Package
UM93520A	16 KHz or 22 KHz by pin option	one 256K DRAM	28L DIP
UM93520AF			48L FP
UM93520B	32 KHz	two 256K DRAMs	28L DIP
UM93520BF			48L FP

General Information

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UMC

Guide To MOS Handling

We at UMC are constantly looking for more effective ways to provide protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Even though oxide breakdown may happen far beyond the voltage levels encountered in normal operation, excessive voltages can cause permanent damage. Though we have evolved the best-designed protective devices currently possible, we recognize that they are not 100-percent effective What is?

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. Careful inspection of the device date sheets and proper pin designation should help reduce such failures.

Gate ruptures caused by static discharge have also accounted for a large percentage of device failures in customers' manufacturing areas. Precautions should be taken to minimize the possibility of static charges during handling and assembly of MOS circuits.

The following guidelines for handling MOS devices are offered to assist our customers in reducing the hazards which may be detrimental to MOS circuits. Precautions listed herein are used at UMC.

A. Cover all benches used for assembly or test of MOS circuits with conductive sheets. Warning: Never expose an operator directly to a hard electrical ground. For safety reasons the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.

B. Have grounding plates on doors and/or floors of all entrances to work areas. These must be contacted by people entering the areas.

C. Have employees wear conductive straps inside and outside their shoes so that body charges are grounded when entering the work area.

D. Have employees wear anti-static neutralized smocks to eliminate the possibility of static charges being generated by the friction of normal wear.

E. Have employees wear cotton gloves while handling parts. Nylon gloves and rubber finger cots are not allowed.

F. To help reduce generation of static voltages, humidity should be controlled at a minimum of 35 percent.

G. Transport all parts in conductive trays. Do not use plastic containers. Store axial leaded parts in conductive foam, e.g. Velofoam #7611.

H. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder pots, reflow soldering equipment, etc.

I. It is advisable to place a grounding clip across the finger of the board to ground all leads and lines on the board during insertion of ICs to printed circuit boards.

J. Use of carpets is discouraged in work areas, but in other areas, carpets may be treated with anti-static solution to reduce static generation.

K. Handle MOS parts on conductive surfaces. The handler must touch the conductive surface first before touching the parts.

L. No power should be applied to the socket or board when the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.

M. Do not handle MOS by their leads unless absolutely necessary. Handle MOS devices by their packages as much as possible.

N. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

Observe these precautions even when an MOS device is suspected of being defective. The real cause of failure cannot be accurately determined if the device is damaged because of static charge build-up.

IMPORTANT REMINDER: EVEN THE MOST ELABORATE PHYSICAL PREVENTION TECHNIQUES WILL NOT ELIMINATE DEVICE FAILURE IF PERSONNEL ARE NOT FULLY TRAINED IN PROPER HANDLING OF MOS DEVICES.

For further information, please contact Quality Assurance/ Reliability Department

United Microelectronics Corp.
No. 10, Innovation First Road,
Science-Based Industrial Park
Hsinchu City, Taiwan, Republic of China

UMC

Quality/Reliability

Design Reliability

Before a new design is approved for production, UMC takes into consideration factors which may affect reliability such as circuit layout, element structures and characteristics, final application, process requirements and assembly, and packaging specs. These aspects are reviewed in the light of quality and reliability standards. Initially, all factors are evaluated on a worst case basis and results are monitored at all stages of the development cycle. These include product planning, layout, mask design, pilot production, testing and packaging. Only when established quality and reliability standards are met in consecutive pilot runs is the product released for production start-up.

Reliability Qualification Tests

The reliability tests include life testing, environmental testing and mechanical testing. These tests are performed in accordance with MIL-STD-883C as the prime standard and with EIAJ-IC-121, where applicable. When a new technique or product is introduced, the UMC reliability engineering department conducts approval and any new process or product is approved only if it meets specified reliability standards and acceptance limits of related tests. Table 1. gives the typical conditions for reliability testing.

Quality Conformance Test

After initial product evaluations are successfully completed, regular testing of volume production is performed on a 100% basis so that test specifications are met in all respects. Additionally, production lots must pass the sampling quality conformance test. Prior to this, the appropriate screening tests are performed on each lot of product.

Engineering Change Control

Engineering approval testing determines the practicality and usability of a process or product.

Production approval is given only if reliability evaluations are successfully met. No device or process change at UMC can be implemented unless full customer notification and approval is received and the change is verified acceptable by the reliability engineering department.

Table 1. Reliability Test Items & Conditions

	Test Items	Test Conditions	Reference Standard	Sample Size	Acc. / Rej.	LTPD
Life Test	Operating Life	T_A=125°C, 1000 hours	MIL-STD-883C 1005.7	55	1/2	7%
	Bias life	T_A=125°C, 1000 hours	MIL-STD-883C 1005.7	55	1/2	7%
	Temperature Humidity with Bias	T_A=85°C, 85% R.H (rated voltage applied) 1000 hours	EIAJ-IC-121 17	55	1/2	7%

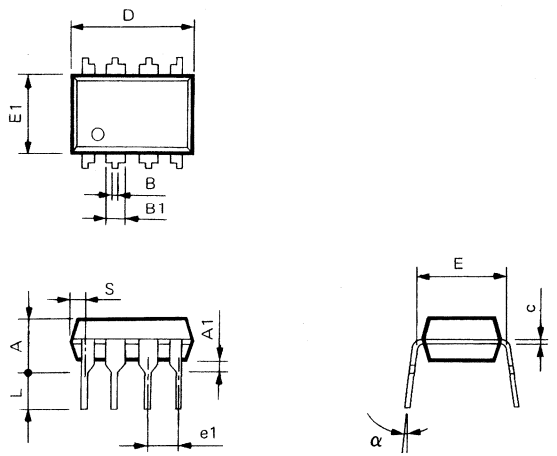
Table 1. Reliability Test Items & Conditions (Continued)

	Test Items	Test Conditions	Reference Standard	Sample Size	Acc. / Rej.	LTPD
Environmental Test	High Temperature Storage	T_A=150°C, 1000 hours	MIL-STD-883C 1008.2	55	1/2	7%
	Low Temperature Storage	T_A=−65°C, 1000 hours	EIAJ-IC-121 16	55	1/2	7%
	Thermal Shock	−65°C ⇌ 150°C 5 min within 10 sec 5 min 100 Cycles	MIL-STD-883C 1011.8	38	1/2	10%
	Temperature Cycling	−65°C ⇌ 150°C 10 min 10 min 200 Cycles	MIL-STD-883C 1010.7	38	1/2	10%
	Pressure Cooker	121°C, 15 psig (2 atm) 100% R.H. 216 hours	EIAJ-IC-121 18	38	1/2	10%
	Salt Atmosphere	35°C, 5% NaCl 24 hours	MIL-STD-883C 1009.8	38	1/2	10%
	Resistance To Soldering Heat	260°C, 10 seconds (Solder Bath)	EIAJ-IC-121 11	15	0/1	15%
Mechanical Test	Lead Fatigue	Bend 90°, 0.229±0.014kg 3 Cycles	MIL-STD-883C 2004.5	15	0/1	15%
	Solderability	230°C + 5°C, 5 seconds Flux used	EIAJ-IC-121 02	15	0/1	15%
	Vibration	100-2000HZ, 20G 4 min/cycle, X.Y.Z Direction	MIL-STD-883C 2007.1	15	0/1	15%
	Mechanical Shock	1500G, 0.5 ms X.Y.Z Direction	MIL-STD-883C 2002.2	15	0/1	15%
	Constant Acceleration	3000G, 60 sec	MIL-STD-883C 2001.2	15	0/1	15%

UMC

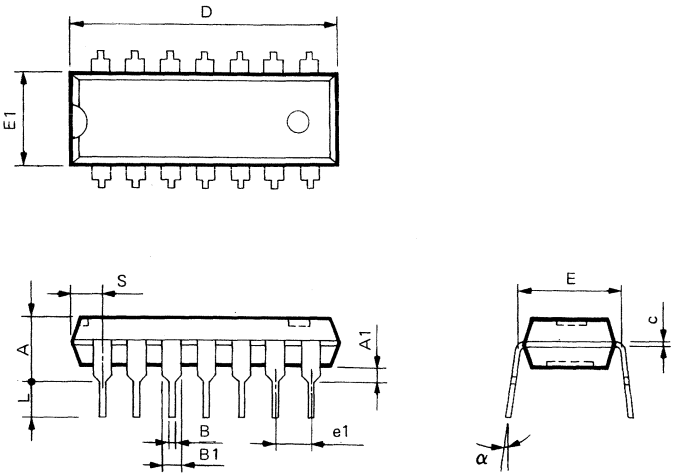
PACKAGING INFORMATION

P- DIP 8L Outline Dimension



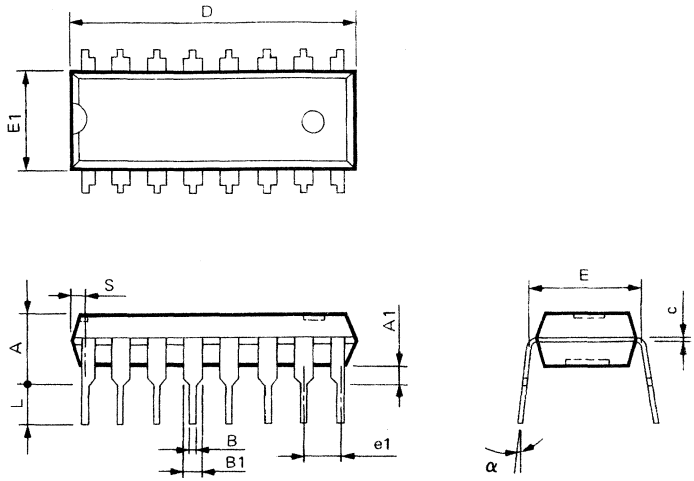
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
B1	0.060 $^{+\ 0.004}_{-\ 0.002}$	1.524 $^{+\ 0.102}_{-\ 0.051}$
c	0.010 $^{+\ 0.004}_{-\ 0.002}$	0.254 $^{+\ 0.102}_{-\ 0.051}$
D	0.360 (0.370 Max.)	9.144 (9.398 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.040 Max.	1.016 Max.

P- DIP 14L Outline Dimension



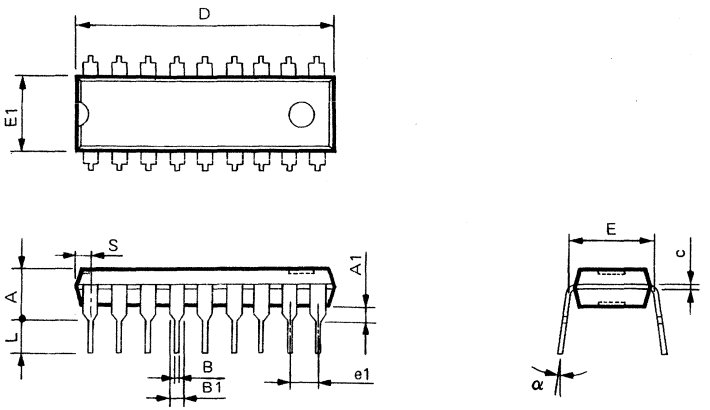
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.060^{+\ 0.004}_{-\ 0.002}$	$1.524^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.750 (0.770 Max.)	19.050 (19.558 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max.

P- DIP 16L Outline Dimension



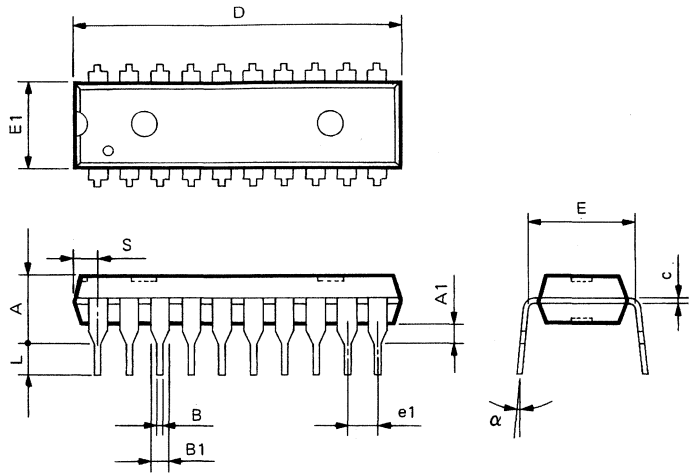
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.750 (0.770 Max.)	19.050 (19.558 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.040 Max.	1.016 Max.

P- DIP 18L Outline Dimension



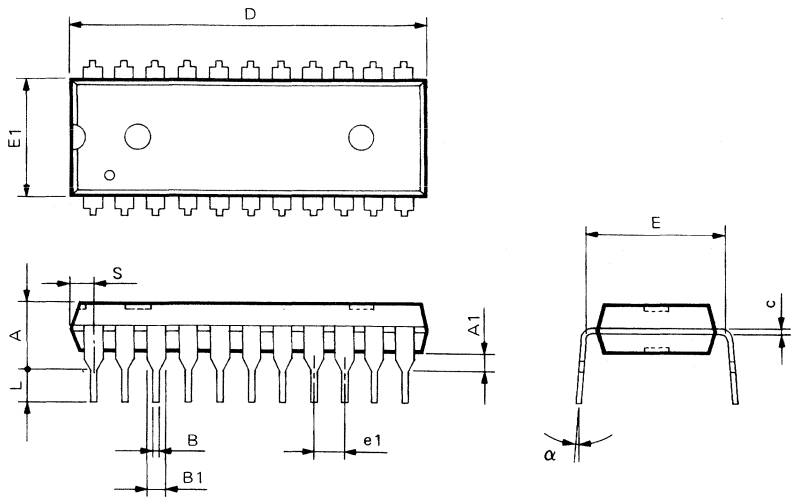
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.900 (0.910 Max.)	22.860 (23.114 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.060 Max.	1.524 Max.

P-DIP 20L Outline Dimension



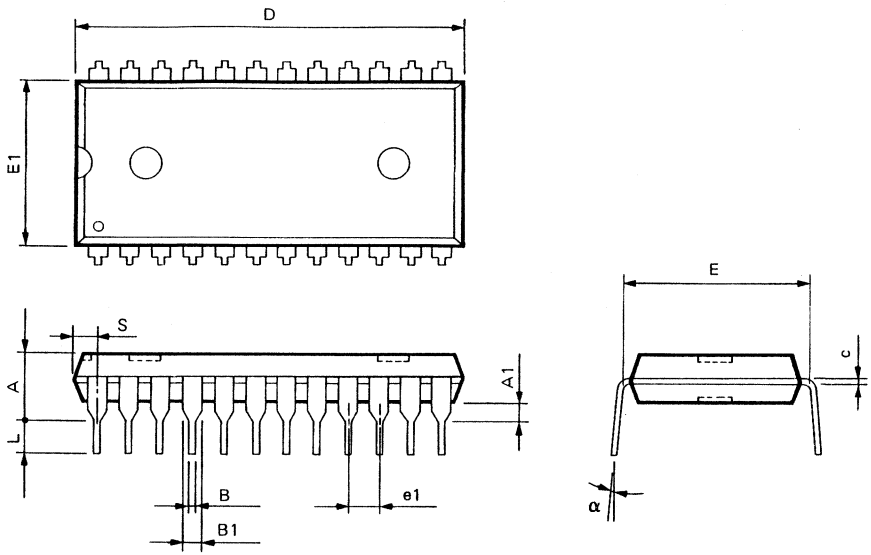
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.026 (1.040 Max.)	26.060 (26.416 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.250 (0.275 Max.)	6.350 (6.985 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.075 Max.	1.905 Max.

P-DIP 22L Outline Dimension



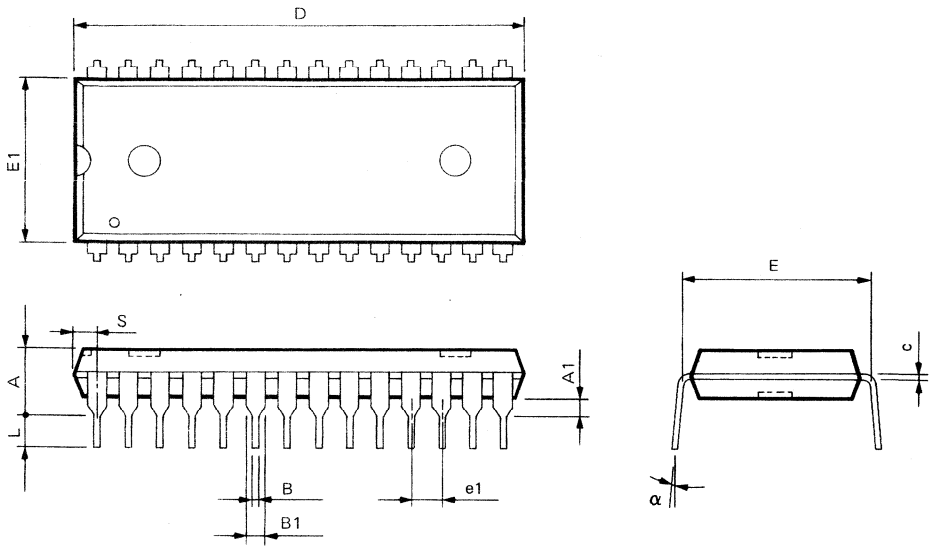
Symbol	Dimensions in inch	Dimensions in mm
A	0.190 max.	4.826 Max.
A1	0.020 Min.	0.508 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.090 (1.120 Max.)	27.686 (28.448 Max.)
E	0.400 ± 0.010	10.160 ± 0.254
E1	0.350 (0.375 Max.)	8.890 (9.525 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.065 Max.	1.651 Max.

P-DIP 24L Outline Dimension



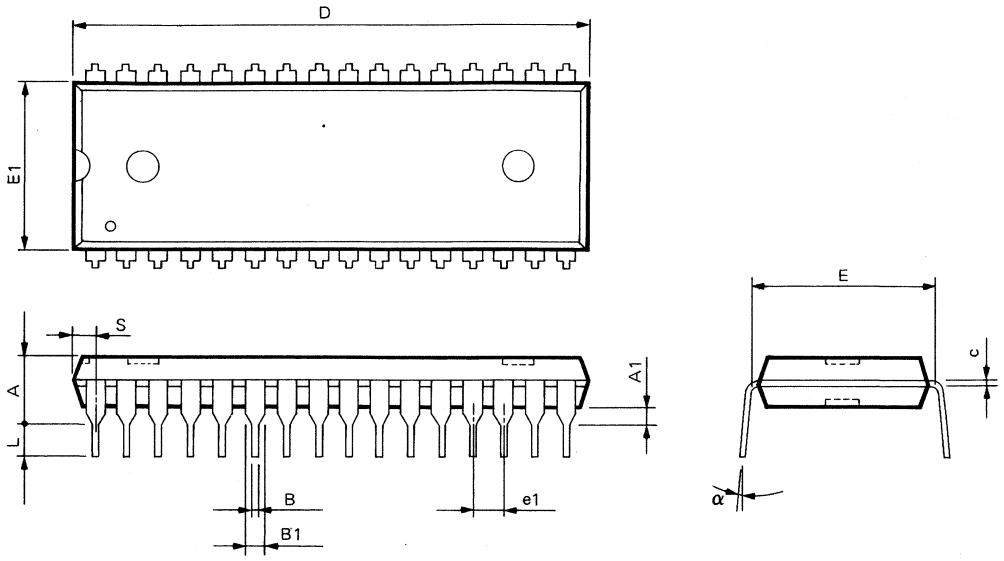
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.250 (1.260 Max.)	31.750 (32.004 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.085 Max.	2.159 Max.

P- DIP 28L Outline Dimension



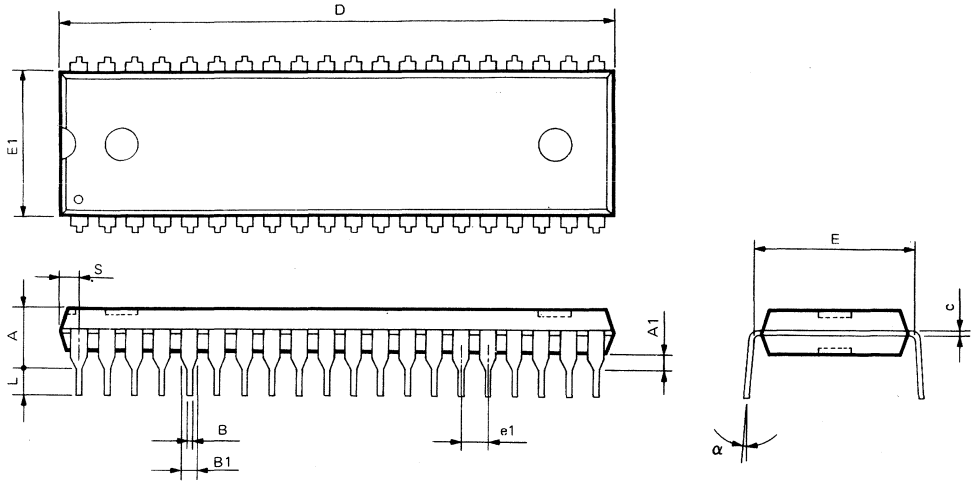
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.060^{+\ 0.004}_{-\ 0.002}$	$1.524^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	1.460 (1.470 Max.)	37.084 (37.338 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.545 (0.575 Max.)	13.843 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max.

P- DIP 32L Outline Dimension



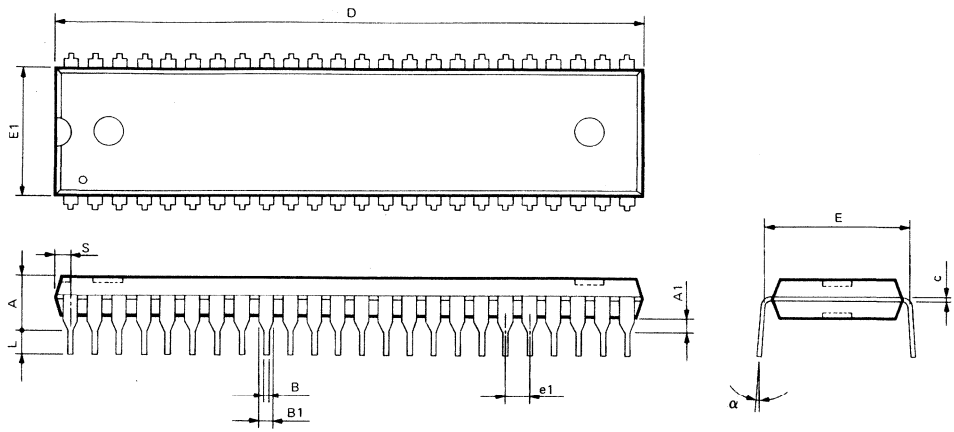
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.050^{+\ 0.004}_{-\ 0.002}$	$1.270^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	1.650 (1.660 Max.)	41.910 (42.164 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.085 Max.	2.159 Max.

P-DIP 40L Outline Dimension



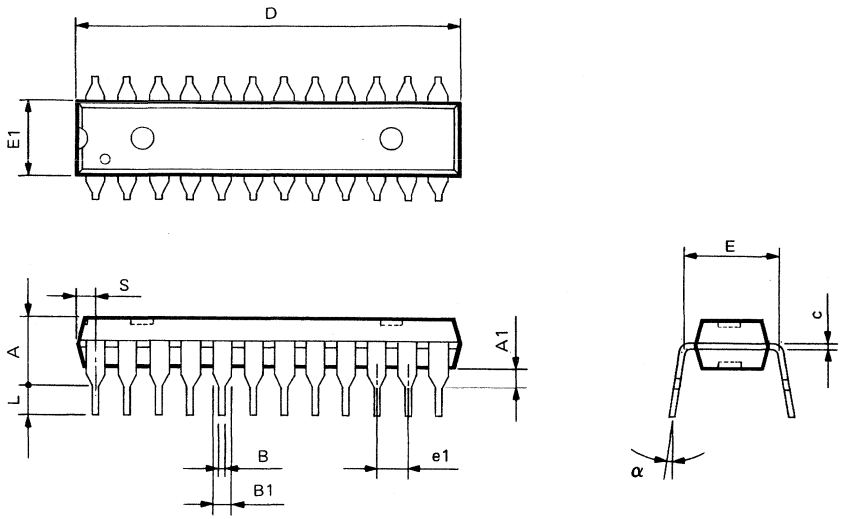
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+\ 0.004}_{-\ 0.002}$	$0.457^{+\ 0.102}_{-\ 0.051}$
B1	$0.050^{+\ 0.004}_{-\ 0.002}$	$1.270^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	2.055 (2.070 Max.)	52.197 (52.578 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max.

P-DIP 48L Outline Dimension



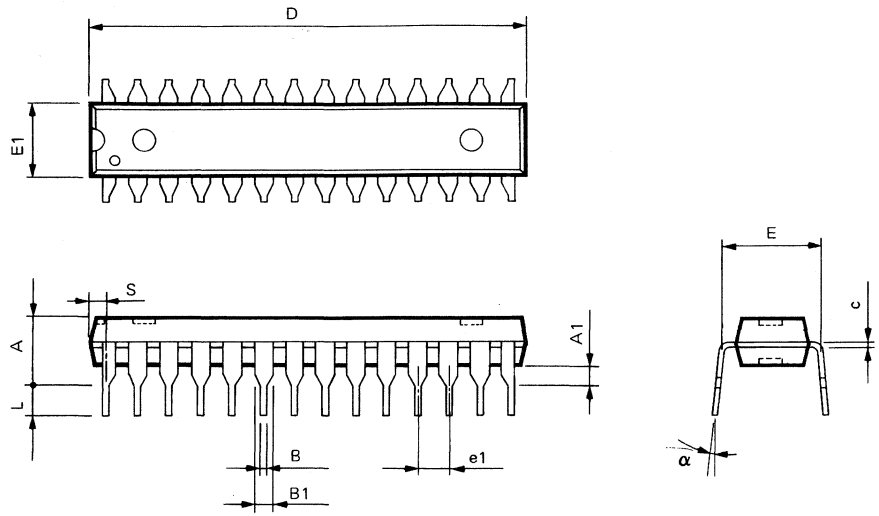
Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.050^{+0.004}_{-0.002}$	$1.270^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	2.450 (2.460 Max.)	62.230 (62.484 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 (0.575 Max.)	13.970 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.085 Max.	2.159 Max.

Skinny 24L Outline Dimension



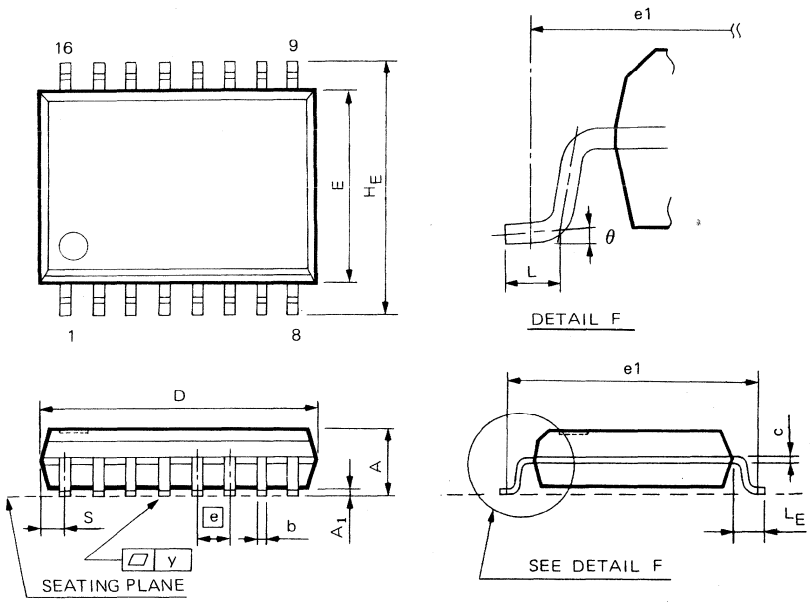
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.256 (1.266 Max.)	31.902 (32.156 Max.)
E	0.300 ± 0.010	7.620 ± 0.254
E1	0.258 (0.285 Max.)	6.553 (7.239 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.088 Max.	2.235 Max.

Skinny 28L Outline Dimension



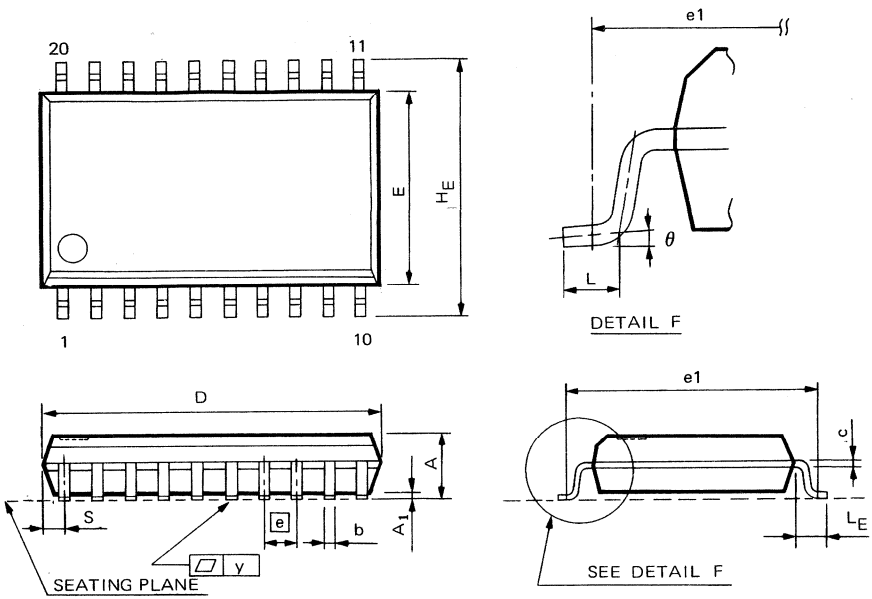
Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max.	4.445 Max.
A1	0.010 Min.	0.254 Min.
B	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
B1	$0.060^{+0.004}_{-0.002}$	$1.524^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	1.388 (1.400 Max.)	35.255 (35.560 Max.)
E	0.310 ± 0.010	7.874 ± 0.254
E1	0.288 (0.310 Max.)	7.315 (7.874 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15	0° ~ 15°
S	0.055 Max.	1.397 Max.

SO 16L Outline Dimension



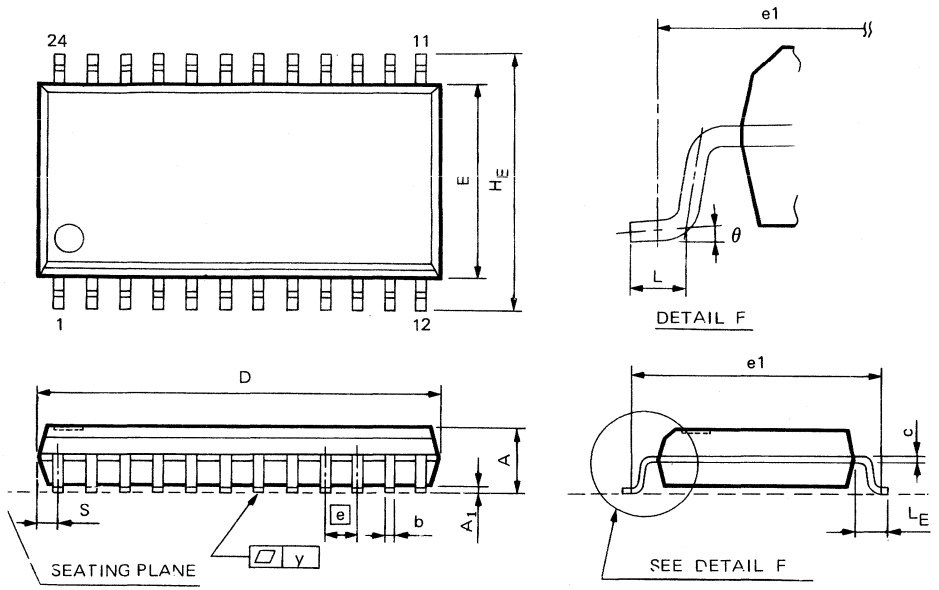
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.405 (0.425 Max.)	10.287 (10.795 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
[e]	0.050 ± 0.006	1.270 ± 0.152
e1	0.374 Nor.	9.50 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.032 ± 0.008	0.813 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.043 Max.	1.092 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 20L Outline Dimension



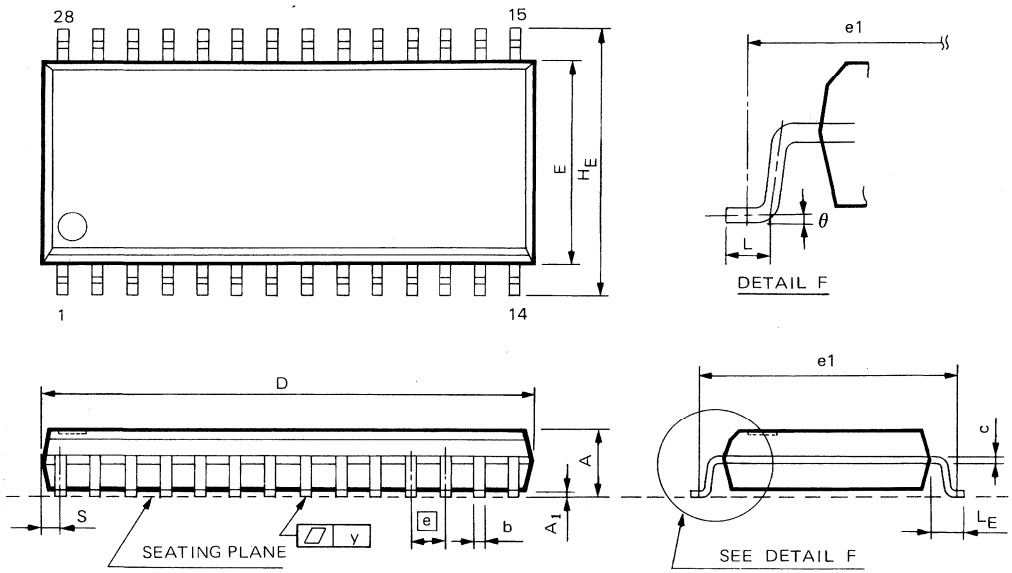
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.504 (0.524 Max.)	12.802 (13.310 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
e1	0.374 Nor.	9.50 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.032 ± 0.008	0.813 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.042 Max.	1.067 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 24L Outline Dimension



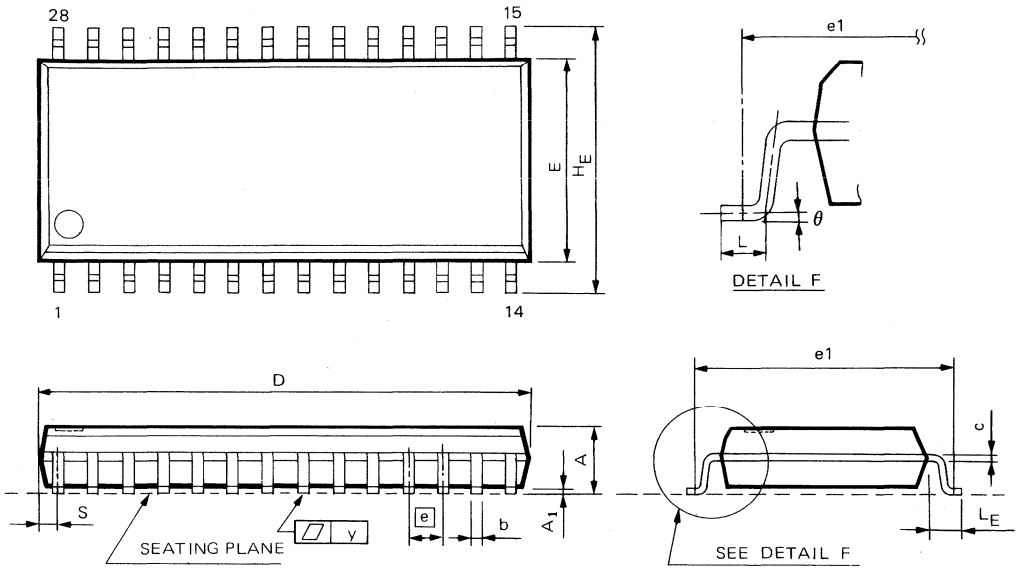
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.006^{+\ 0.004}_{-\ 0.002}$	$0.152^{+\ 0.102}_{-\ 0.051}$
D	0.606 (0.611 Max.)	15.392 (15.520 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
[e]	0.050 ± 0.006	1.270 ± 0.152
e1	0.370 Nor.	9.40 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.036 ± 0.008	0.914 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.035 Max.	0.889 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 28L Outline Dimension (300 mil)



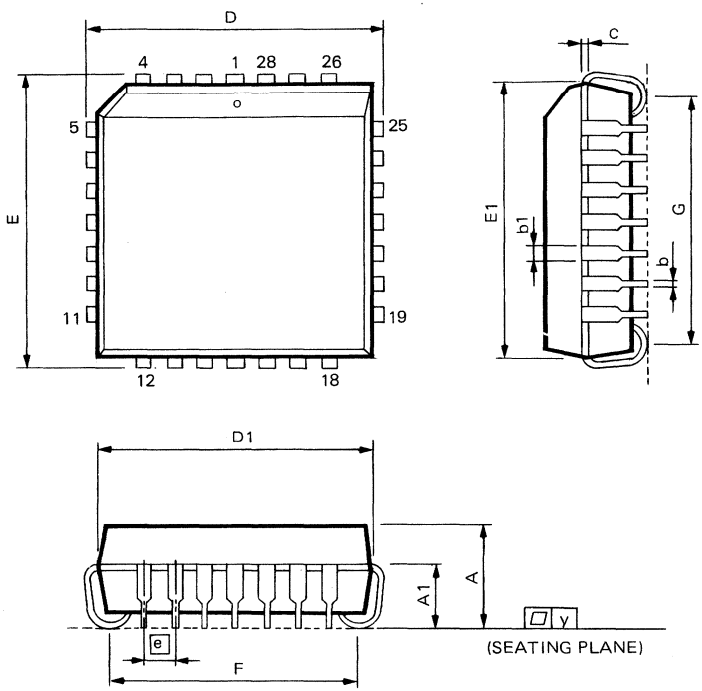
Symbol	Dimensions in inch	Dimensions in mm
A	0.106 Max.	2.692 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.705 (0.730 Max.)	17.907 (18.540 Max.)
E	0.295 (0.320 Max.)	7.493 (8.128 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
e1	0.370 Nor.	9.40 Nor.
H_E	0.406 ± 0.010	10.312 ± 0.254
L	0.036 ± 0.008	0.914 ± 0.203
L_E	0.055 ± 0.008	1.397 ± 0.203
S	0.045 Max.	1.143 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

SO 28L Outline Dimension (330 mil)



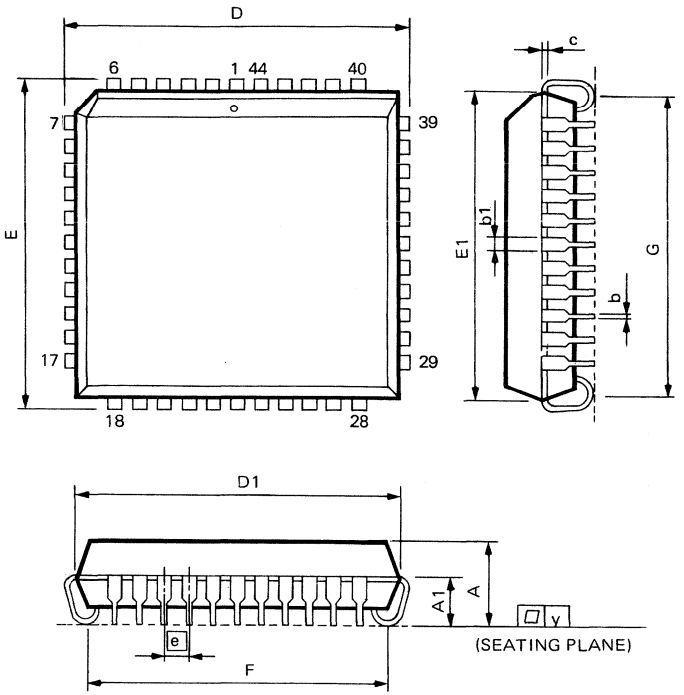
Symbol	Dimensions in inch	Dimensions in mm
A	0.112 Max.	2.845 Max.
A1	0.004 Min.	0.102 Min.
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.406^{+\ 0.102}_{-\ 0.051}$
c	$0.010^{+\ 0.004}_{-\ 0.002}$	$0.254^{+\ 0.102}_{-\ 0.051}$
D	0.713 (0.736 Max.)	18.110 (18.694 Max.)
E	0.331 (0.356 Max.)	8.407 (9.042 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
e1	0.429 Nor.	10.90 Nor.
H_E	0.465 ± 0.010	11.811 ± 0.254
L	0.036 ± 0.008	0.914 ± 0.203
L_E	0.067 ± 0.008	1.702 ± 0.203
S	0.048 Max.	1.219 Max.
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

PLCC 28L Outline Dimension



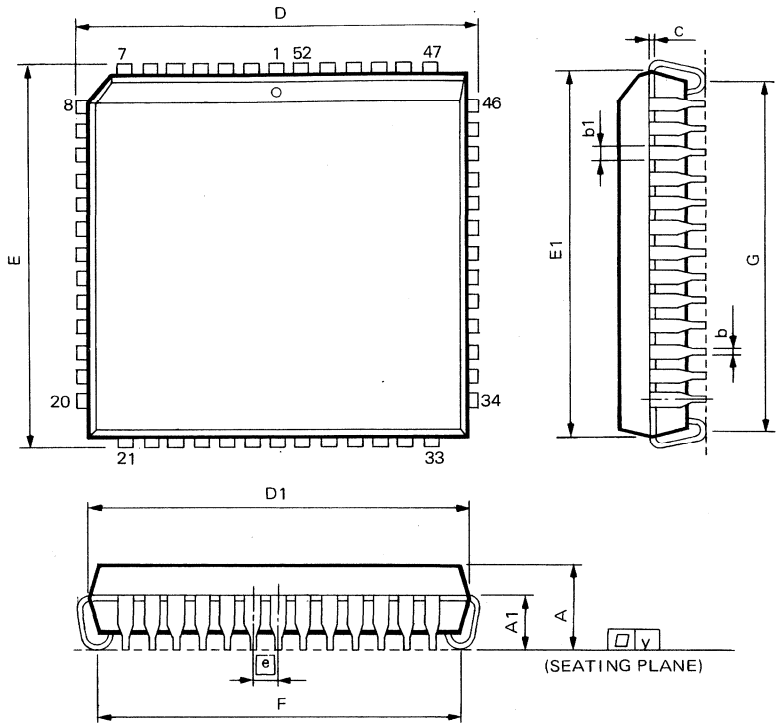
Symbol	Dimensions in inch	Dimensions in mm
A	0.172 ± 0.008	4.369 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	$0.018^{+0.004}_{-0.002}$	$0.457^{+0.102}_{-0.051}$
b1	$0.028^{+0.004}_{-0.002}$	$0.711^{+0.102}_{-0.051}$
c	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.490 ± 0.005	12.446 ± 0.127
D1	0.453 (0.485 Max.)	11.506 (12.319 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	0.490 ± 0.005	12.446 ± 0.127
E1	0.453 (0.485 Max.)	11.506 (12.319 Max.)
F	0.410 ± 0.020	10.414 ± 0.508
G	0.410 ± 0.020	10.414 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 44L Outline Dimension



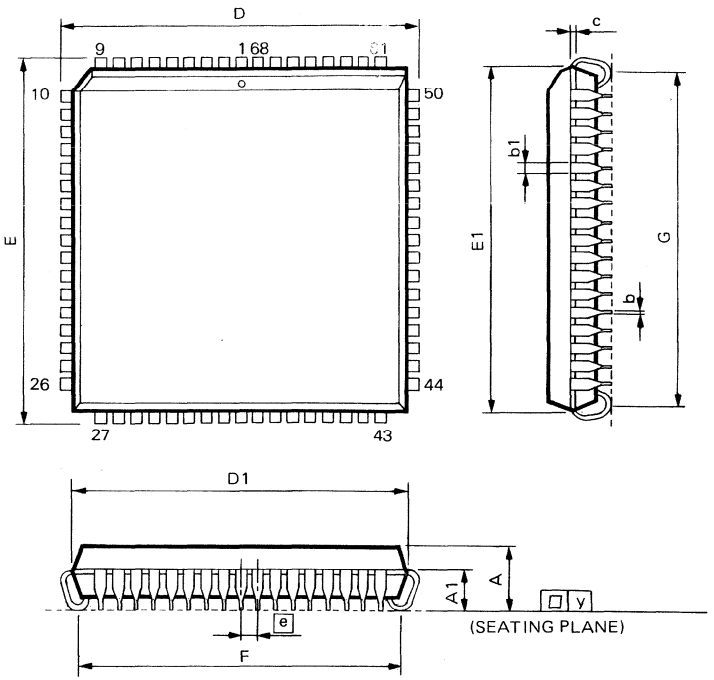
Symbol	Dimensions in inch	Dimensions in mm
A	0.172 ± 0.008	4.369 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.010 $^{+\ 0.004}_{-\ 0.002}$	0.254 $^{+\ 0.102}_{-\ 0.051}$
D	0.690 ± 0.005	17.526 ± 0.127
D1	0.653 (0.685 Max.)	16.586 (17.399 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	0.690 ± 0.005	17.526 ± 0.127
E1	0.653 (0.685 Max.)	16.586 (17.399 Max.)
F	0.615 ± 0.020	15.621 ± 0.508
G	0.615 ± 0.020	15.621 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 52L Outline Dimension



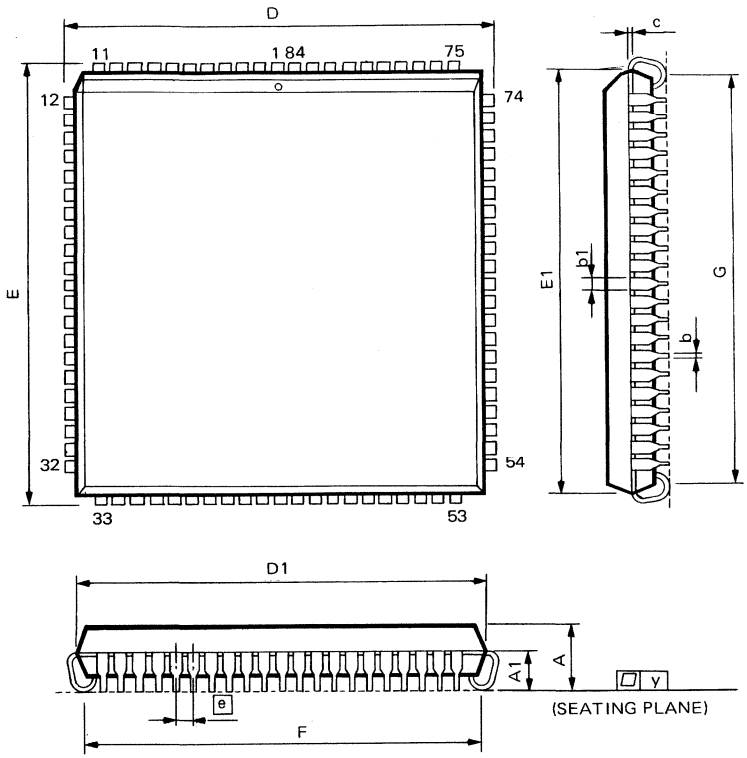
Symbol	Dimensions in inch	Dimensions in mm
A	0.172 ± 0.008	4.369 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.010 $^{+\ 0.004}_{-\ 0.002}$	0.254 $^{+\ 0.102}_{-\ 0.051}$
D	0.790 ± 0.005	20.066 ± 0.127
D1	0.753 (0.785 Max.)	19.126 (19.939 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	0.790 ± 0.005	20.066 ± 0.127
E1	0.753 (0.785 Max.)	19.126 (19.939 Max.)
F	0.710 ± 0.020	18.034 ± 0.508
G	0.710 ± 0.020	18.034 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 68L Outline Dimension



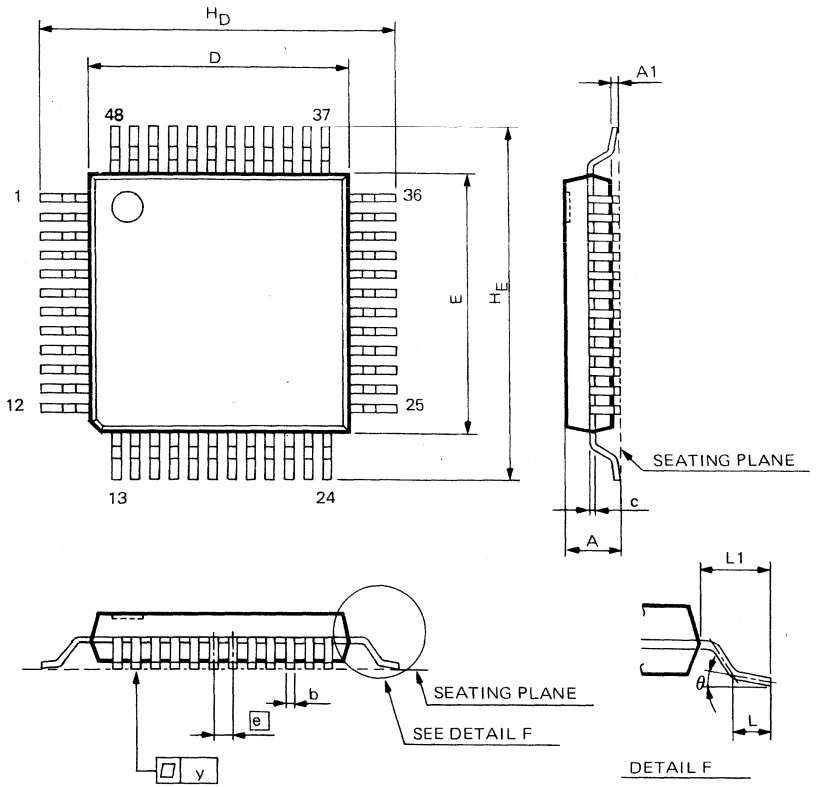
Symbol	Dimensions in inch	Dimensions in mm
A	0.170 ± 0.008	4.318 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.008 $^{+\ 0.004}_{-\ 0.002}$	0.203 $^{+\ 0.102}_{-\ 0.051}$
D	0.990 ± 0.005	25.146 ± 0.127
D1	0.954 (0.985 Max.)	24.232 (25.019 Max.)
e	0.050 ± 0.006	1.275 ± 0.152
E	0.990 ± 0.005	25.146 ± 0.127
E1	0.954 (0.985 Max.)	24.232 (25.019 Max.)
F	0.917 ± 0.020	23.292 ± 0.508
G	0.917 ± 0.020	23.292 ± 0.508
y	0.006 Max.	0.152 Max.

PLCC 84L Outline Dimension



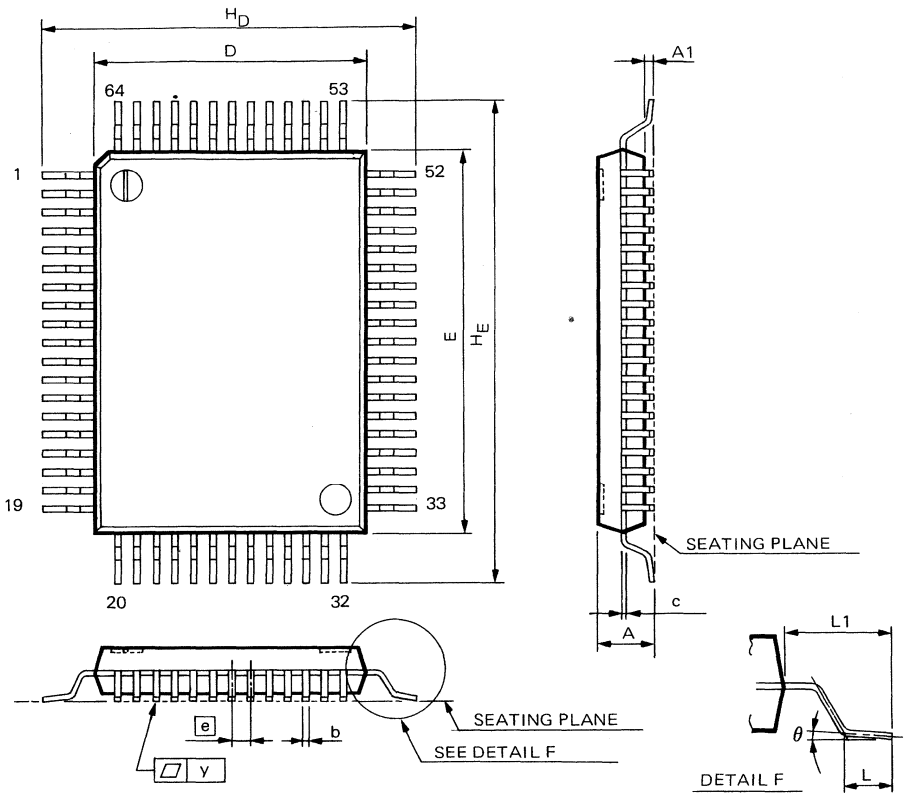
Symbol	Dimensions in inch	Dimensions in mm
A	0.170 ± 0.008	4.318 ± 0.203
A1	0.100 ± 0.008	2.540 ± 0.203
b	0.018 $^{+\ 0.004}_{-\ 0.002}$	0.457 $^{+\ 0.102}_{-\ 0.051}$
b1	0.028 $^{+\ 0.004}_{-\ 0.002}$	0.711 $^{+\ 0.102}_{-\ 0.051}$
c	0.008 $^{+\ 0.004}_{-\ 0.002}$	0.203 $^{+\ 0.102}_{-\ 0.051}$
D	1.190 ± 0.005	30.226 ± 0.127
D1	1.153 (1.185 Max.)	29.286 (30.099 Max.)
e	0.050 ± 0.006	1.270 ± 0.152
E	1.190 ± 0.005	30.226 ± 0.127
E1	1.163 (1.185 Max.)	29.286 (30.099 Max.)
F	1.117 ± 0.020	28.372 ± 0.508
G	1.117 ± 0.020	28.372 ± 0.508
y	0.006 Max.	0.152 Max.

QFP 48L Outline Dimension



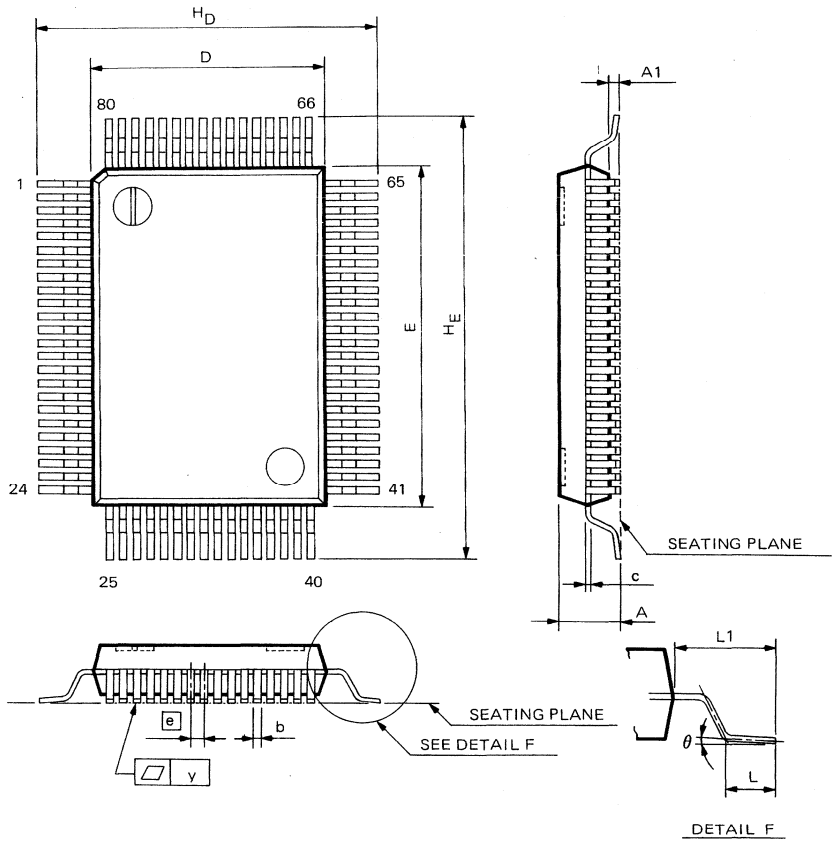
Symbol	Dimensions in inch	Dimensions in mm
A	0.063 ± 0.012	1.600 ± 0.305
A1	0.006 ± 0.004	0.152 ± 0.102
b	0.013 $^{+\ 0.004}_{-\ 0.002}$	0.330 $^{+\ 0.102}_{-\ 0.051}$
c	0.006 $^{+\ 0.004}_{-\ 0.002}$	0.152 $^{+\ 0.102}_{-\ 0.051}$
D	0.394 (0.420 Max.)	10.000 (10.668 Max.)
E	0.394 (0.420 Max.)	10.000 (10.668 Max.)
e	0.030 ± 0.006	0.762 ± 0.152
H_D	0.630 ± 0.014	16.000 ± 0.356
H_E	0.630 ± 0.014	16.000 ± 0.356
L	0.075 ± 0.012	1.905 ± 0.305
L1	0.118 ± 0.012	2.997 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

QFP 64L Outline Dimension



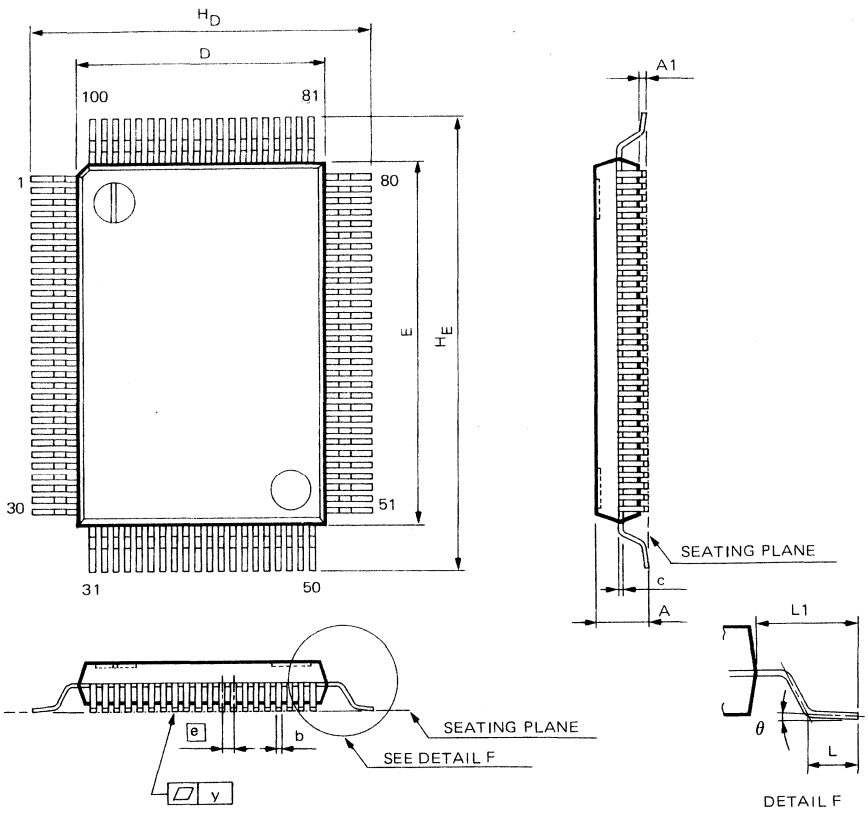
Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.016^{+\ 0.004}_{-\ 0.002}$	$0.400^{+\ 0.102}_{-\ 0.051}$
c	$0.006^{+\ 0.004}_{-\ 0.002}$	$0.152^{+\ 0.102}_{-\ 0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
e	0.039 ± 0.006	1.000 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

QFP 80L Outline Dimension



Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.014^{+0.004}_{-0.002}$	$0.351^{+0.102}_{-0.051}$
c	$0.006^{+0.004}_{-0.002}$	$0.152^{+0.102}_{-0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
e	0.032 ± 0.006	0.800 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
y	0.006 Max.	0.152 Max.
θ	0° ~ 8°	0° ~ 8°

QFP 100L Outline Dimension



Symbol	Dimensions in inch	Dimensions in mm
A	0.120 ± 0.010	3.048 ± 0.254
A1	0.008 ± 0.004	0.203 ± 0.102
b	$0.012^{+\ 0.004}_{-\ 0.002}$	$0.305^{+\ 0.102}_{-\ 0.051}$
c	$0.006^{+\ 0.004}_{-\ 0.002}$	$0.152^{+\ 0.102}_{-\ 0.051}$
D	0.551 (0.576 Max.)	14.000 (14.630 Max.)
E	0.787 (0.812 Max.)	20.000 (20.625 Max.)
e	0.026 ± 0.006	0.650 ± 0.152
H_D	0.740 ± 0.012	18.796 ± 0.305
H_E	0.976 ± 0.012	24.790 ± 0.305
L	0.047 ± 0.012	1.194 ± 0.305
L1	0.095 ± 0.012	2.413 ± 0.305
y	0.006 Max.	0.152 Max.
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QPS ELECTRONICS, INC.(NF)
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AVED ELECTRONICS, INC. (F)
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BELL MICROPRODUCTS (F)
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OMNI PRO (F)
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FAX: 214-385-7508

OMNI PRO (F)
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